**IEEE P802.15**

**Wireless Personal Area Networks**

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| Project | IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs) |
| Title | **D2 Comments Resolution Based Offset-VPWM PHY/MAC Specification Revision** |
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| Re: | Draft D2 Comment Resolution based Offset-VPWM PHY/MAC Specification Revision |
| Abstract | Details of Resolutions regarding to the submitted Comments on D2 are suggested for Offset-VPWM PHY/MAC Specification Revision. The PHY IV Offset-VPWM is designed to operate on the application services like LED ID, LiFi/CamCom, Digital Signage with Advertisement Information etc. |
| Purpose | Draft D2 Comments Resolutions and Editorial Revision. |
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# **1. PHY IV SUPERFRAME STRUCTURE**

# **4.9.1 Offset-VPWM Superframe Structure**

The Offset Variable Pulse Width Modulation for Smart Device Flash Light PHY uses the unslotted ALOHA; that is, when the Smart Device flash light transmitter has a packet to send, it just transmit the data. This support with beacon and without beacon support and the transmitter does not do a listen before talk channel activity check.

# **2. PHY IV DIMMING**

**8.5.2.4.2 Offset-VPWM dimming**

In the Offset Variable Pulse Width Modulation for Smart Device Flash Light uses the Smartphone Camera LED Flash light sources and no need to concern about dimming. The Camera LED Flash light is not using for illumination and blinking speed is very low, then can't control dimming.

The Figure 166 shows the 2bit symbol map flickering control for Offset Variable Pulse Width Modulation for Smart Device Flash Light.



**Figure 166 – 2 Bit Symbol Flickering Control**

In accordance with the provisions of the symbol, depending on the data bit transmission because the High Pulse interval being determined brightness is adjustable (P >> V, V>time error (jitter)).

# **3. PHY IV PPTU Format**

**8.6.1.2.2 Offset-VPWM Preamble Field**

The preamble field is used by the transceiver to obtain optical clock synchronization with an incoming message. The standard defines one fast locking pattern (FLP). The MAC shall select the optical clock rate for communication during the clock rate selection process. The preamble shall be sent at a clock rate chosen by the TX and supported by the RX. The preamble is a time domain sequence and does not have any channel coding or line coding.

The preamble first starts with a FLP. The FLP is fixed as a pattern “11010010”. The fast locking pattern length shall not exceed the maximum. The timing information for preamble is shown in Figure 181.



**Figure 181 – Preamble Timing Diagram**

In the Offset Variable Pulse Width Modulation for Smart Device Flash Light PHY uses OOK modulation for preamble transmission using flash light. The Preamble Bit Mapping shown in Figure 182.



**Figure 182 – Preamble Transmission – OFFSET VPWM BIT MAPPING**

**8.6.5.2.2 Offset-VPWM PSDU field**

The PSDU field has a variable length and carries the data of the PHY IV frame. The FCS is appended if the PSDU has a non-zero byte payload. The structure of the PSDU field is as shown in Figure 191.



**Figure 191 – Offset-VPWM PHY PSDU Field Structure**

# **4. PHY SPECIFICATIONS FOR OFFSET-VPWM**

**13.5 Offset-VPWM**

**13.5.1 OFFSET-VPWM PHY Specifications**

The Offset-VPWM PHY supported data rates and operating conditions is shown in Table 114 – PHY IV Operating Modes for Offset Variable Pulse Width Modulation.

The proposed Offset-VPWM (Variable Pulse Width Modulation) designed with following characteristics,

* Modulation methods includes line coding
* Defining the sum (P + nV) of the unit to be added to the minimum pulse (P) which is a reference pulse width (V) as a Symbol ( P>>V, V>time error(jitter) )
* Can specify a 2bit data symbol, 4bit data symbol according to number of added pulse
* Data is expressed with offset pulse width, 2bits data(for example) were mapped into 4 Offset-VPWM symbols

The data symbol map for two bits symbol with pulse width and respective symbol blinking waveform are shown in Table 192 and Figure 243 respectively.



**Table 192 – Two Bits Symbol Mapping Truth Table**

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**Figure 243 – Two Bit Symbol Data Diagram**

In offset-VPWM, the data is expressed with offset pulse width, 4bits data (for example) were mapped into 16 Offset-VPWM symbols. The 4 bits symbol mapping truth table is shown in Table 193.



 **Table 193 – Four Bits Symbol Mapping Truth Table**

The symbol arrays mapping is described in waveform pattern as shown in Figure 244.



**Figure 244 – Symbol Array Mapping Timing Diagram**

# **5. PHY IV SUPERFRAME STRUCTURE**

**5.2.1.8 Frame Payload field**

**5.2.1.8.2 PHY IV**

**Frame Payload Field**

The Frame Payload field has a variable length and contains information specific to individual frame types. If the Security Enabled subfield is set to one in the frame control field, the frame payload is protected as defined by the security suite selected for that frame.

**5.2.1.9 FCS field**

**5.2.1.9.2 PHY IV**

The FCS field is 2 octets in length and the FCS is calculated over the MHR and MSDU parts of the frame. The FCS shall be only generated for payloads greater than zero bytes. The FCS is option is given as an optional option, it is adaptive to RS/CRC/NONE.

The FEC supported methods for Offset VPWM is given in Table XXX.

|  |  |  |
| --- | --- | --- |
| **No** | **RS Method**  | **RS Rate** |
| 1 | None | 1 |
| 2 | RS(15,2) | 2/15 |
| 3 | RS(15,4) | 4/15 |

**Table XXX – Offset VPWM FEC Outer Code Support**

**6. RECEIVER DECODING FOR OFFSET-VPWM**

**Annex G (Informative)**

**OFFSET-VPWM Receiver Processing Guide**

**G.1 Receiver Detection Method**

The offset-VPWM receiver can synchronize rising edge and check pulse width length using Rolling-shutter method. The receiver detection process in the wave formatted approach is show in Figure 373.



**Figure 373 – Receiver Detection Process**