**IEEE P802.15**

**Wireless Personal Area Networks**

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| Project | IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs) | |
| Title | **2D-invisible sequential code** | |
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| Abstract | [PHY and MAC specification for 2D-invisible sequential code] | |
| Purpose | [PHY and MAC specification of 2D-invisible sequential code for draft-D0-text-input] | |
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**PHY Layer Operating mode(s)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PHY Operating Modes** | | | | |
| **Modulation**  **(m:n)** | **RLL Code** | **Optical Clock Rate** | **FEC** | **Data Rate (bits)**  **m x n x 15 x FEC\_rate** |
| 2D-invisible sequential code 4:3 | None | 30Hz | FEC\_option | 180 x FEC\_rate |
| 2D-invisible sequential code 16:10 | None | 30Hz | FEC\_option | 2400 x FEC\_rate |
| 2D-invisible sequential code 8:5 | None | 30Hz | FEC\_option | 600 x FEC\_rate |
| 2D-invisible sequential code 16:9 | None | 30Hz | FEC\_option | 2160 x FEC\_rate |
| 2D-invisible sequential code 8:3 | None | 30Hz | FEC\_option | 360 x FEC\_rate |

N: Number of vertical cells

M: Number of horizontal cells

FEC\_option: Select one FEC scheme from Table 1

FEC\_rate: the data rate scale of FEC scheme

Figure 1 shows an example of cell configuration on display device with M=4 and N=3.

N=3



M=4

Figure 1. Example of cell construction

Table 1: FEC option

|  |  |  |
| --- | --- | --- |
| FEC\_option | FEC description | FEC\_rate |
| 1 | none | 1 |
| 2 | RS(64,32) | 1/2 |
| 3 | RS(160,128) | 128/160 |
| 4 | RS(15,7) | 5/7 |
| 5 | RS(15,11) | 11/15 |
| 6 | RS(15,2) | 2/15 |
| 7 | RS(15,4) | 4/15 |
| 8 | RS(15,7) | 7/15 |
| 9 | CC(1/4) | 1/4 |
| 10 | CC(1/3) | 1/3 |
| 11 | CC(2/3) | 2/3 |

**2.0 PHY specifications**

2.1 Reference modulator diagram

The reference implementation diagram is in Figure 2.

Data

Serial to parallel

Display data

Encoder

Display device

FEC encoder

Figure 2. Reference modulator diagram

The image framing order for n x m bits data encoding is shown in Figure 3.

n x m bits data

Serial to parallel

Encoder

Reference image

m x n bits embedded image

FEC encoder

Figure 3. Image frame order

2.2 Invisible sequential code Encoder

The encoded bits in display cell are defined as:

Logic zero: represented by the unchanged sensitive element of color space.

Logic one: represented by the changed sensitive element of color space.

An example of logic bit encoding is shown in Figure 4.

Reference display



Modulated display

Figure 4. Example of modulated image frame with 110001000010 bits stream. (a. Reference image. b. Modulated image)

# PHY Layer Dimming Method

Invisible sequential code can support dimming by changing the brightness of display image. The brightness does not affect the invisible element of reference image and embedded image. The reference diagram is shown by Figure 5.

Data

Serial to parallel

Display data

Encoder

Display device

FEC encoder

Dimming level

Figure 5 Reference modulator diagram with dimming control data

1. **PPDU format**

The PPDU frame structure shall be formatted as illustrated in Figure 6.

PSDU

PHY header

Preamble

SHR

PHY payload

PHR

Figure 6Format of the PPDU

4.1 Preamble Field

The synchronization of one superframe data based on 2 mark image frames as Figure 7. Length of preamble field varies from 24 to 380 bits. It depends on the operation mode.



Synchronization 1

Synchronization 2



Figure 7 Preamble frame

4.2 PHY header

The PHY header, as shown in Table 2, defines the data length of data payload.

Table 2.

|  |  |  |
| --- | --- | --- |
| PHY header fields | Bit-width | Explanation on usage |
| PSDU length | 8 | Length up to aMaxPHYFrameSize |
| FEC\_option | 8 | Provide information about FEC option |

4.3 PSDU field

The PSDU field has a variable length and carries the data of the PHY frame.

**5.0 PHY PIB attributes**

**6.0 Superframe Structure**

Invisible sequential code is applied for broadcasting mode. There is no access control mechanism. There is no superframe.

**7.0 MAC frame formats**

The MAC frame contains only frame Payload. The length of frame Payload is defined by PSDU length value of PHY header.

**8.0 MAC PIB attributes**