**IEEE P802.15**

**Wireless Personal Area Networks**

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[12a PHY specification for HRCP 3](#_Toc429736032)

[12a.1 General requirements 3](#_Toc429736033)

[12a.1.1 Regulatory Information 3](#_Toc429736034)

[12a.1.2 RF power measurements 3](#_Toc429736035)

[12a.1.3 Unwanted emissions 3](#_Toc429736036)

[12a.1.4 RF channelization 3](#_Toc429736037)

[12a.1.5 Transmit PSD mask 3](#_Toc429736038)

[12a.1.6 HRCP PHY Management 4](#_Toc429736039)

[12a.2 HRCP-SC PHY 6](#_Toc429736040)

[12a.2.1 PHY operating specifications of HRCP-SC PHY 6](#_Toc429736041)

[12a.2.1.1 Channelization 6](#_Toc429736042)

[12a.2.2 Modulation and coding 6](#_Toc429736043)

[12a.2.2.1 MCS dependent parameters 6](#_Toc429736044)

[12a.2.2.2 Header dependent parameters 7](#_Toc429736045)

[12a.2.2.3 Timing-related parameters 7](#_Toc429736046)

[12a.2.2.4 Frame-related parameters 7](#_Toc429736047)

[12a.2.2.5 Modulation 8](#_Toc429736048)

[12a.2.2.6 Forward Error Correction 9](#_Toc429736049)

[12a.2.2.7 Stuff bits 10](#_Toc429736050)

[12a.2.2.8 Code spreading 11](#_Toc429736051)

[12a.2.2.9 Scrambling 11](#_Toc429736052)

[12a.2.3 HRCP-SC PHY frame format 11](#_Toc429736053)

[12a.2.3.1 PHY preamble 11](#_Toc429736054)

[12a.2.3.1.1 Frame synchronization (SYNC) 12](#_Toc429736055)

[12a.2.3.1.2 Start frame delimiter (SFD) 12](#_Toc429736056)

[12a.2.3.1.3 Channel estimation sequence (CES) 12](#_Toc429736057)

[12a.2.3.2 Frame Header 13](#_Toc429736058)

[12a.2.3.2.1 HRCP-SC PHY header 13](#_Toc429736059)

[12a.2.3.2.2 Header HCS 14](#_Toc429736060)

[12a.2.3.2.3 Header FEC 15](#_Toc429736061)

[12a.2.3.3 HRCP-SC PHY Payload field 16](#_Toc429736062)

[12a.2.3.3.1 HRCP-SC PHY Payload scrambling 16](#_Toc429736063)

[12a.2.3.3.2 Modulation 16](#_Toc429736064)

[12a.2.3.3.3 FEC 16](#_Toc429736065)

[12a.2.3.4 Pilot word and PCES 16](#_Toc429736066)

[12a.2.3.4.1 Subblocks and pilot word 16](#_Toc429736067)

[12a.2.3.4.2 PCES 16](#_Toc429736068)

[12a.2.4 Transmitter specifications 16](#_Toc429736069)

[12a.2.4.1 Error Vector Magnitude 16](#_Toc429736070)

[12a.2.4.2 Symbol rate 17](#_Toc429736071)

[12a.2.4.3 Transmit power-on and power-down ramp 17](#_Toc429736072)

[12a.2.5 Receiver specifications 17](#_Toc429736073)

[12a.2.5.1 Error rate criterion 17](#_Toc429736074)

[12a.2.5.2 Receiver sensitivity 17](#_Toc429736075)

[12a.2.5.3 Receiver maximum input level 18](#_Toc429736076)

[12a.2.6 PHY layer timing 18](#_Toc429736077)

[12a.2.6.1 Interframe space 18](#_Toc429736078)

[12a.2.6.2 Receive-to-transmit turnaround time 18](#_Toc429736079)

[12a.2.6.3 Transmit-to-receive turnaround-time 18](#_Toc429736080)

[12a.2.6.4 Time between successive transmissions 19](#_Toc429736081)

[12a.2.6.5 Channel switch 19](#_Toc429736082)

[12a.2.7 PHY management for HRCP-SC PHY 19](#_Toc429736083)

[12a.2.7.1 Maximum frame size 19](#_Toc429736084)

[12a.2.7.2 Maximum transfer unit size 19](#_Toc429736085)

[12a.2.7.3 Minimum fragment size 19](#_Toc429736086)

[12a.2.8 MIMO, channel bonding and channel aggregation 19](#_Toc429736087)

[12a.3 HRCP-OOK PHY 20](#_Toc429736088)

***Insert the following clause as Clause 12a:***

# 12a PHY specification for HRCP

## General requirements

A compliant HRCP PHY shall implement at least one of the following PHY modes:

a) HRCP single carrier mode PHY (HRCP-SC PHY), as defined in 12a.2.

b) HRCP on-off keying mode PHY (HRCP-OOK PHY), as defined in 12a.3.

Unless otherwise stated, in all figures in this clause the ordering of the octets and bits as they are presented to the PHY for modulation is the same as defined in 7.1.

### Regulatory Information

The HRCP PHY operating frequency is within the 57.0–66.0 GHz range as allocated by the regulatory agencies in Europe, Japan, Canada, and the United States. This band will also be available in other areas where allocated by the regulatory bodies.

The documents listed in Table 94 are provided as a reference for various geographic regulatory regions. The list is neither exhaustive nor complete. It is the responsibility of the implementer to verify that the DEV complies with all regulatory requirements in the geographic region where the device is deployed or sold.

The maximum allowable output power, as measured in accordance with practices specified by the appropriate regulatory bodies, is shown in Table 95. A compliant DEV may use any transmit power level up to the applicable limits in the geographical region.

### RF power measurements

Unless otherwise stated, all RF power measurements for the purpose of this standard, either transmit or receive, shall be made based on EIRP and any radiated measurements shall be corrected to compensate for the antenna gain in the implementation. The gain of the antenna is the maximum estimated gain by the manufacturer.

### Unwanted emissions

Conformant implementations shall comply with the in-band and out-of-band emissions for all operational modes as set by the applicable regulatory bodies.

### RF channelization

The HRCP PHY uses the channels defined in Table XX.

A channel aggregation is defined in 12a.2.1.1.

The channel whose CHNL\_ID is 2 shall be defined as default channel.

### Transmit PSD mask

The transmitted spectrum for HRCP PHY using a single channel shall adhere to the transmit spectrum mask shown in Figure XX. For the transmit mask measurements, the resolution bandwidth is set to 3 MHz and video bandwidth to 300 kHz. During OOK modulation, transmitters shall meet the same PSD mask, except for the single line spectra of 40 dB above the 0 dB line in Figure XX within the frequency band of [–6 MHz,+6 MHz] from the carrier frequency.

The transmitted spectrum for a channel bonding is defined in Figure XX.



**Figure XX—Transmit spectral mask**

### HRCP PHY Management

The PHY dependent PIB values for the HRCP PHY are given in Table XXX and Table XXX. The PHY PIB characteristics group, Table XX, contains information that is common to most implementations.

**Table XXX -PHY PIB characteristics group parameters**

|  |  |  |  |
| --- | --- | --- | --- |
| **Manged Object** | **Octets** | **Definition** | **Access** |
| PHYPIB\_Type | 1 | 0x02 = HRCP PHY | Read/Write |
| PHYPIB\_Type | 1 | bit 1 = HRCP-SC PHYbit 2 = HRCP-OOK PHYbit 3-8 = ReservedA bit is set to one if the associated PHY is supported, and is set to zero otherwise. | Read/Write |
| PHYPIB\_RegDomainsSupported | Variable | One octet for each regulatory domain supported, as defined for PHYPIB\_CurrentRegDomain. | Read/Write |
| PHYPIB\_CurrentRegDomain | 1 | 0x00 = European Telecommunications Standards Institute (ETSI)0x01 = Federal Communications Commission (FCC)0x02 = Industry Canada (IC)0x03 = Association of Radio Industries and Businesses (ARIB) | Read/Write |
| PHYPIB\_DataRateVector | Variable | One octet for each supported MCS. The msb indicates the HRCP PHY mode, as in PHYPIB\_Mode, and the last seven lsbs contain the MCS supported for that mode using the encoding for that PHY mode. | Read/Write |
| PHYPIB\_NumChannelsSupported | Variable | Value = 0x04, as defined in 12a.1.4. | Read/Write |
| PHYPIB\_CurrentChannel | 1 | Indicates the channel that is currently being used, asdefined in 12a.1.4. | Read/Write |
| PHYPIB\_FrameLengthMax | 2 | pMaxFrameBodySize. | Read/Write |

The PHY PIB implementation group, Table XXX contains information that is more characteristic of a particular PHY implementation than of the PHY as a whole.

**Table XXX—PHY PIB implementation group parameters**

|  |  |  |  |
| --- | --- | --- | --- |
| **Manged Object** | **Octets** | **Definition** | **Access** |
| PHYPIB\_DiversitySupported | 1 | Numeric entry that indicates the number of antennas that are available. | Read/Write |
| PHYPIB\_MaxTXPower | 1 | The maximum TX power that the DEV is capable of using, 7.4.11, implementation dependent. | Read/Write |
| PHYPIB\_TXPowerStepSize | 1 | The step size for power control supported by the DEV, 7.4.12, implementation dependent. | Read/Write |
| PHYPIB\_NumPMLevels | 1 | Number of power management levels supported. The range is 1 to 8 and the value is implementation dependent.  | Read/Write |
| PHYPIB\_PMLevelReturn | Variable | Table of vectors with number of entries given by PHYPIB\_NumPMLevels. Each vector is the time required to change between power saving states of the PHY. Vector number 0 is the time required to change the PHY from the off state to a state where it is ready to receive commands. Other values are implementation dependent.  | Read/Write |

## HRCP-SC PHY

The HRCP-SC PHY is designed for extremely high PHY-SAP payload-bit rates between 2 Gb/s and 13 Gb/s using a single channel with a band width of 2.16 GHz and the maximum 100 Gb/s using multiple input, multiple output (MIMO), a channel aggregation and a channel bonding.

The HRCP-SC PHY supports π/2-shift BPSK, π/2-shift QPSK, 16-QAM, 64-QAM and 256-QAM modulations. The modulation of π/2-shift BPSK is just used for preamble and header sequences, and other modulations are used for a payload. The modulations of π/2-shift BPSK and π/2-shift QPSK are mandatory for HRCP-SC PHY and other modulations are optional.

FEC scheme is specified by two LDPC codes with a code rate of 14/15 and a code rate of 11/15. These two LDPC codes are mandatory for HRCP-SC PHY

The HRCP-SC PHY also supports the channel aggregation, channel bonding and MIMO. The channel aggregation, channel bonding and MIMO are optional.

### PHY operating specifications of HRCP-SC PHY

#### Channelization

The RF channels are defined in Table XX. A compliant implementation shall support at least 1 channel from the channels allocated for operation by its corresponding regulatory body.

A channel aggregation uses a combination of separated two channels, *i*.*e*. CHNL\_IDs 1 & 3, 1 & 4, and 2 & 4.

The PHYPIB\_CurrentChannel is the CHNL\_ID of the current channel. For the purpose of the Remote Scan Request and Remote Scan Response commands, as described in 7.5.7.3 and 7.5.7.4, respectively, the Channel Index field is the CHNL\_ID in Table XX.

### Modulation and coding

#### MCS dependent parameters

The chip rate for all HRCP-SC PHY MCS is given in Table XX. The MCS dependent parameters shall be set according to Table XX. The data rates in the table are approximate and are calculated to three significant figures.

**Table xx—MCS dependent parameters**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **MCS identifier** | **modulation** | **FEC rate** | **data rate (Gb/s)****w/ PW** | **data rate (Gb/s)****w/o PW** |
| 0 | π/2-shift QPSK | 11/15 | 2.5813  | 2.2587  |
| 1 | π/2-shift QPSK | 14/15 | 3.2853  | 2.8747  |
| 2 | 16-QAM | 11/15 | 5.1627  | 4.5173  |
| 3 | 16-QAM | 14/15 | 6.5707  | 5.7493  |
| 4 | 64-QAM | 11/15 | 7.7440  | 6.7760  |
| 5 | 64-QAM | 14/15 | 9.8560  | 8.6240  |
| 6 | 256-QAM | 14/15 | 13.1413  | 11.4987  |

A subblock length for HRCP-SC PHY shall be 128 chips. The pilot word (PW) length for HRCP-SC PHY shall be 0 or 16 chips. The PW length of 0 is mandatory and that of 16 chips is optional.

#### Header dependent parameters

The header dependent parameters shall be set according to Table XXX. The headers use an extended Hamming (EH) code, as defined in 12a.2.3.2.3.

**Table XXX—** **Header rate dependent parameters**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Header rate (Mb/s)** | **Moudlation Scheme** | **Spreading Factor, LSF** | **FEC** | **Pilot word length (chips), LPW** | **Code bits per subblock, LCBPS** | **Number of occupied subblocks, Nsubblock\_hdr** | **Number of stuff bits, LSTUFF** |
| 162 | /2-shift BPSK | 4 | EH | 8 | 14 | 19 | 40 |

#### Timing-related parameters

Table XXX lists the general timing parameters associated with the SC PHY.

**Table XXX—Timing-related parameters**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Parameter** | **Description** | **Value** | **Unit** | **Formula** |
| *R*c | Chip rate | 1760 | Mchip/s |  |
| *T*C | Chip duration | ~0.568 | ns | 1/*R*C |
| *L*subblock | Subblock length | 64 | chips |  |
| *L*PW | Pilot word length | 0 | 8 | chips |  |
| *T*PW | Pilot word duration | 0 | 4.5 | ns |  |
| *L*DC | Length of dat chips per subblock | 64 | 56 | chips |  |
| *T*subblock | Subblock duration | ~36.4 | ns | *L*subblock×*T*c |
| *R*subblock | Subblock rate | 27.5 | MHz | 1/ *T*subblock |

#### Frame-related parameters

The frame parameters associated with the PHY are listed in Table XXX where CEIL is the ceiling function, which returns the smallest integer value greater than or equal to its argument. The maximum frame duration occurs when the number of octets in the PHY Payload field is 524288.

**Table XXX—Frame-related parameters**

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Description** | **Value** |
| *N*SYNC | Number of code repititions in the SYNC sequence | 14 |
| *T*SYNC | Duration of the SYNC sequence | ~1 µs |
| *N*SFD | Number of code repetitions in SFD | 1 |
| *T*SFD | Duration of the SFD | ~0.07 µs  |
| *N*CES | Number of code repetitions i the CES | 11 |
| *T*CES | Duration of the CES | ~0.8 µs |
| *N*pre | Number of code repetitions in the PHY preamble | 26 |
| *T*pre | Duration of the PHY preamble | ~1.89 µs  |
| *L*hdr | Length of the header in octets | 14 |
| *N*subblock\_hdr | Number of subblocks in the base frame header | CEIL[*L*hdr × 8 × *L*SF / (*L*subblock *–* *L*PW)] |
| *T*hdr | Duration of the base frame header | *N*subblock\_hdr × *T*subblock |
| *L*payload | Length of frame payload in octets | Variable |
| *L*FCS | Length of FCS in octest | 4 |
| *L*CBPS | Number of coded bits per subblock in the MAC frame body | (*L*subblock *–* *L*PW) / *L*SF |
| *Nsubblock\_MFB* | Number of subblocks in the MAC frame body | CEIL[(*L*MFB × 8) / (*R*FEC × *L*CBPS)] |
| *T*MFB | Duration of the MAC and PHY frame body | *N*subblock\_MFB × *T*subblock |
| *T*frame | Duration of the frame | *T*pre + *T*hdr + *T*datafield |

#### Modulation

After channel encoding and spreading, the bits shall be inserted into the constellation mapper.

The constellations of π/2-shift BPSK, pre-coded (G)MSK, π/2-shift QPSK used for the HRCP-SC PHY are the same as illustrated in Figure 164 (a), (b), and (c), respectively, in 12.2.2.5.1 and 12.2.2.5.2. The constellations of 16QAM and 64QAM used for the HRCP-SC PHY are the same as illustrated in Figure 183 in12.3.2.

The constellation map of 256QAM used for the HRCP-SC PHY is illustrated in Figure xx. The serial bit stream shall be divided into groups of four bits with input bit *d*1 being the earliest in the stream.

The normalization factor for 256-QAM constellation is 1/Sqrt(170). An approximate value of the normalization factor may be used, as long as the device conforms to the modulation accuracy requirements.



**Figure xx—Constellation map of 256 QAM**

#### Forward Error Correction

The forward error correction (FEC) schemes are specified in this subclause. Supporting the following two rate-compatible LDPC codes, *i*.*e*. a rate-14/15 LDPC(1440,1344) code and a rate-11/15 LDPC(1440,1056) code, are mandatory for HRCP-SC PHY.

Although the rate-14/15 LDPC(1440,1344) code is defined in 12.2.2.6.3, the two LDPC code is simultaneously defined here as following.

The LDPC codes are systematic, *i*.*e*. the LDPC encoder encodes an information block of length *k*, **i** = (*i*0, *i*1, …, *ik*–1), into a codeword **c** of length 1440, **c** = (*i*0, *i*1, …, *ik*–1, *p*0, *p*1, …, *p*1440–*k*–1), by adding (1440– *k*)parity bits (*p*0, *p*1, …, *p*1440–*k*–1) obtained so that **Hc***T* = 0, where **H** is an (1440– *k*) × 1440parity-check matrix and *T* denotes transverse operation. Denote the parity check matrix as **H** = (*hi,j*), where *hi,j* consists of {0,1}, 0 ≤ *i <*(1440– *k*) and 0 ≤ *j <* 1440.

Table I lists the parameters of the LDPC codes with a codeword length of 1440, *e*.*g*. supported code rates, information-block lengths *k* and parity lengths, and the matrix elements whose values are ‘1’ in the first 15 columns of parity check matrix **H** with 1440 columns for the LDPC codes.

**Table XXX—Parameters of the LDPC codes with a codeword length of 1440**

|  |  |  |
| --- | --- | --- |
| code rate | 14/15 | 11/15 |
| information-block length, *k* (bits) | 1344 | 1056 |
| parity length (bits) | 96 | 384 |
| matrix elements whose values are ‘1’ in the first 15 columns of parity check matrix **H** | *h*0,0 *h*1,0 *h*4,0 | *h*96,0 *h*193,0 *h*4,0 |
| *h*32,1 *h*34,1 *h*39,1 | *h*34,1 *h*320,1 *h*135,1 |
| *h*64,2 *h*70,2 *h*78,2 | *h*352,2 *h*70,2 *h*270,2 |
| *h*8,3 *h*18,3 *h*95,3 | *h*104,3 *h*306,3 *h*287,3 |
| *h*31,4 *h*42,4 *h*54,4 | *h*31,4 *h*234,4 *h*150,4 |
| *h*63,5 *h*76,5 *h*91,5 | *h*159,5 *h*364,5 *h*91,5 |
| *h*14,6 *h*45,6 *h*94,6 | *h*302,6 *h*45,6 *h*286,6 |
| *h*30,7 *h*47,7 *h*83,7 | *h*126,7 *h*239,7 *h*371,7 |
| *h*17,8 *h*62,8 *h*80,8 | *h*17,8 *h*158,8 *h*272,8 |
| *h*28,9 *h*48,9 *h*82,9 | *h*28,9 *h*336,9 *h*178,9 |
| *h*22,10 *h*60,10 *h*81,10 | *h*214,10 *h*60,10 *h*369,10 |
| *h*27,11 *h*49,11 *h*84,11 | *h*219,11 *h*145,11 *h*372,11 |
| *h*7,12 *h*53,12 *h*77,12 | *h*7,12 *h*245,12 *h*173,12 |
| *h*19,13 *h*44,13 *h*85,13 | *h*19,13 *h*140,13 *h*373,13 |
| *h*6,14 *h*46,14 *h*75,14 | *h*6,14 *h*238,14 *h*363,14 |

For 15 ≤ *j*, the matrix element can be obtained by using Equation (xx).

*hi,j* = *h*96\*floor(*i*/96) + mod(*i* + floor(*j*/15), 96), mod(*j*, 15), (xx)

where mod(*x*, *y*) is the modulo function and is defined as (*x* – *n*×*y*), where *n* is the nearest integer less than or equal to *x*/*y*.

Each LDPC code is a quasi-cyclic code such that every cyclic shift of a codeword by 15 symbols yields another codeword.

For shortened LDPC operation, the *k–l* zero elements are appended to the incoming *l* message bits as follows: *ri* = 0 for *i* = *l*, *l*+1, …, *k*–1. The message order is *rk*–1 as the first bit of the message with *r*0 as the last bit of the message. These inserted zero elements are not transmitted.

#### Stuff bits

Stuff bits shall be added to the end of the encoded MAC frame body if the number of the encoded data bits is not an integer multiple of the length of the data portion in the subblock. The number of stuff bits is computed for each subframe if standard aggregation is employed. The calculation of stuff bits is as follows.

In the encoded MAC frame body, the number of FEC codewords, *NFEC* is given by Equation (xx).

*NFEC* = CEIL[(*LMFB* × 8)/(1440× *RFEC*)], (xx)

where *LMFB* is the length of the MAC frame body in octets, and *RFEC* isthe FEC rate.

The encoded MAC frame body shall be concatenated with stuff bits of length *LSTUFF* so that the resulting

MAC frame body is aligned on the subblock symbol boundary. The stuff bits shall be set to zero and then

scrambled using the continuation of the scrambler sequence that scrambled the MAC frame body in

12a.2.2.10. The length of bits in the encoded MAC frame body, *Lebits* is given by Equation (xx).

*Lebits* = 8 × *LMFB* + *NFEC* × (1 – *RFEC*) × 1440(xx)

#### Code spreading

To increase robustness in header, pseudo random binary sequence (PRBS) codes by linear feedback shift register (LFSR) are applied for code spreading.

PRBS generation with LFSR is described in Figure 168.

#### Scrambling

The frames shall be scrambled by modulo-2 addition of the data with the output of a PRBS generator, as illustrated in Figure 168 with *LSF* = 1.

### HRCP-SC PHY frame format

The HRCP-SC PHY frame shall be formatted as illustrated in Figure 172.

The Frame Header field for the PHY frame shall be formatted as illustrated in Figure XXX

|  |  |
| --- | --- |
| Stuff bits | header-FEC encoded |
| scrambled | PHY Header |
| HCS | MAC Header |

**Figure XXX—Frame header format**

The PHY preamble is described in 12a.1.9.1. The MAC header is defined in 7.2. The PHY header is defined in 12a.2.3.2.1, and the HCS is defined in 12a.2.3.2.2. The header FEC is defined in 12a.2.3.2.3. The PHY Payload field consisting of the MAC frame body, the PCES and stuff bits, is described in 12a.2.3.3. The PCES is described in 12a.2.3.4.2. The stuff bits are described in 12a.2.2.7.

#### PHY preamble

A PHY preamble shall be added prior to the frame header to aid receiver algorithms related to auto-gain control (AGC) setting, frame detection, timing acquisition, frequency offset estimation, frame synchronization and channel estimation.

The PHY preamble, *i*.*e*. PHY-long preamble and PHY-short preamble, shall be transmitted at the chip rate 1760MHz.

A PHY-long preamble shall be used for the beacon frame defined in Figure 15a in 7.3.1.2a.

A PHY-short preamble shall be used for the payload.

Figure XXX shows the structure of the PHY-long or PHY-short preambles.

For PHY preamble, TSFD is 0.07 µs and TCES is 0.80 µs. For PHY-long preamble, TSYNC is 1.45 µs and TPRE is 2.33 µs. For PHY-short preamble, TSYNC is 1.02 µs and TPRE is 1.89 µs.



**Figure XXX—HRCP-SC PHY preamble structure**

##### Frame synchronization (SYNC)

The SYNC field is used for frame detection and uses a repetition of codes for a higher of robustness. The SYNC field for PHY-long preamble shall consist of 20 code repetitions of **a**128. The SYNC field for PHY-short preamble shall consist of 14 code repetitions of **a**128. Table XX shows the sequence **a**128 used for the SYNC field. The lsb of the **a**128 shall be transmitted first.

**Table XXX—Golay sequences with length 128**

|  |  |
| --- | --- |
| **Sequence name**  | **Sequence value** |
| **a**128 | 5A5599963C33FFF00F00CCC36966AAA5 |
| **b**128 | A5AA6669C3CC000F0F00CCC36966AAA5 |

##### Start frame delimiter (SFD)

The SFD field is used to establish frame timing. The SFD field shall consist of the sign inversion sequence of **a**128.

##### Channel estimation sequence (CES)

The CES field, used for channel estimation, shall consist of [**a**256 **b**512 **a**512 **b**128] where the right most sequence, **b**128, is first in time. The sequence **b**128 is defined in Table XXX and the lsb of the **b**128 shall be transmitted first.

The Golay complementary sequences of length 512, denoted by **a**512 **b**512, are defined as:

**a**512 = [**b**256 **a**256],

**b**512 = [–**b**256 **a**256],

where the number on the right **a**256 are the first in time.

The Golay complementary sequences of length 256, denoted by **a**256 **b**256, are defined as:

**a**256 = [**b**128 **a**128],

**b**256 = [–**b**128 **a**128],

where the number on the right **a**128 are the first in time.

#### Frame Header

A frame header shall be added after the PHY preamble. The frame header conveys information in the PHY

and MAC headers necessary for successfully decoding the frame. The frame header consists of a base frame header followed by an optional frame header. The construction of the frame header is shown in Figure 175.

The detailed process of the construction is as follows:



**Figure XXX—Frame header construction process**

a) Form the frame header as follows

1. Construct the PHY header based on information provided by the MAC
2. Compute the HCS over the combined PHY and MAC headers
3. Append the HCS to the MAC header
4. Scramble the combined MAC header and HCS, as described in 12.2.2.10
5. Encode the concatenation of the PHY header, scrambled MAC header and scrambled HCS into a concatenated extended hamming codes, as described in 12a.2.3.2.3
6. Form the base frame header by concatenating the coded PHY header, coded scrambled MAC header, coded scrambled HCS, and scrambled stuff bits

The resulting frame header shall be modulated as shown in Figure 175.

b) Spread the frame header, as described in 12.1.12.2.

c) Map the frame header onto /2 BPSK, as described in 12.2.2.5.1.

d ) Build subblocks from the resulting frame header, as described in 12.2.3.4.1.

The LFSR for the spreader is reset between the header and payload.

##### HRCP-SC PHY header

The HRCP-SC PHY header shall be formatted as illustrated in Figure XXX.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **bits:19** | **5** | **4** | **1** | **3** |
| Frame length | Reserved | Scrambler seed ID | Pilot word | MCS |

**Figure XXX—** **PHY header format for HRCP-SC PHY**

The MCS field shall be set according to the values in Table XXX.

The Pilot Word field shall be set to one if the pilot word used in the current frame and shall be set to zero if otherwise.

The Scrambler Seed ID field contains the scrambler seed identifier value, as defined in 12.2.2.10.

The Frame Length field shall be an unsigned integer equal to the number of octets in the MAC frame body of a regular frame, excluding the FCS.

**Table XXX—** **Modulation and coding scheme**

|  |  |
| --- | --- |
| **MCS** | **MCS identifier** |
| 000 | 0 |
| 001 | 1 |
| 010 | 2 |
| 011 | 3 |
| 100 | 4 |
| 101 | 5 |
| 110 | 6 |
| 111 | reserved |

##### Header HCS

The combination of the PHY header and MAC header shall be protected with a CRC-16 header check sequence (HCS). The MAC parameter, pLengthHCS shall be 2 for this PHY. The CRC-16 HCS shall be the ones complement of the remainder generated by the modulo-2 division of the protected combined PHY and MAC headers by the polynomial

x16+x15+x13+x8+x5+x3+x+1 (XXX)

The protected bits shall be processed in transmit order. All HCS calculations shall be made prior to data scrambling. A schematic of the processing is shown in Figure XXX.

**Figure XXX—CRC-16** Implementation

##### Header FEC

To increase robustness in the frame header, the combination of the PHY header, scrambled MAC header and HCS shall be encoded to concatenated code words of an extended hamming code.

For each 4-bit input sequence, denoted as {i0, i1, i2, i3}, the encoder shall output the sequence followed by a 4-bit-parity sequence, denoted as {p0, p1, p2, p3} determined using Table XXX.

**Table XXX—Parity assignment of the Header FEC**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **i0** | **i1** | **i2** | **i3** | **p0** | **p1** | **p2** | **p3** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

#### HRCP-SC PHY Payload field

The HRCP-SC PHY Payload field is the last component of the frame, and is constructed as shown in Figure 177.

The PHY Payload field shall be constructed as follows:

1. Scramble the MAC frame body according to 12.2.2.10.
2. Encode the scrambled MAC frame body as specified in 12a.2.2.6.
3. Add stuff bits to the encoded and scrambled MAC frame body according to 12a.2.2.7.
4. Map the resulting MAC frame body onto the appropriate constellation as described in 12a.2.2.5.
5. Build subblocks from the resulting MAC frame body according to 12a.2.3.4.1.
6. Insert PCES periodically as described in 12a.2.3.4.2.

##### HRCP-SC PHY Payload scrambling

The HRCP-SC PHY payload shall use the scrambling process defined in 12.2.2.10

##### Modulation

Modulation for the MAC frame body is defined in 12a.2.2.5.

##### FEC

FEC for the MAC frame body is defined in 12a.2.2.6.

#### Pilot word and PCES

##### Subblocks and pilot word

Subblocks and pilot word are defined in 12.2.3.4.1.

##### PCES

TBD

### Transmitter specifications

#### Error Vector Magnitude

A compliant transmitter shall have EVM values of less than –14 dB.

#### Symbol rate

The SC PHY shall be capable of transmitting at the chip rate, as defined in Table 107, to within ±25 s/s.

The MAC parameter, pPHYClockAccuracy, shall be ±25 s/s.

#### Transmit power-on and power-down ramp

The transmit power-on ramp is defined as the time it takes for the RF power emitted by the compliant DEV to rise from less than 10% to greater than 90% of the maximum power to be transmitted in the frame.

The transmit power-on ramp shall be less than 9.3 ns.

The transmit power-down ramp is defined as the time it takes for the RF power emitted by the compliant DEV to fall from greater than 90% to less than 10% of the maximum power to be transmitted in the frame.

The transmit power-down ramp shall be less than 9.3 ns.

The transmit power ramps shall be constructed such that the emissions conform to the unwanted emissions specification defined in 12a.1.3.

### Receiver specifications

#### Error rate criterion

The error rate criterion shall be a frame error rate (FER) of less than 8% with a frame payload length of 214 octets. The error rate should be determined at the PHY SAP interface after any error correction methods

(excluding retransmission) required in the proposed device has been applied. The measurement shall be

performed in AWGN channel.

#### Receiver sensitivity

The receiver sensitivity is the minimum power level of the incoming signal, in dBm, present at the input of the receiver for which the error rate criterion in 12a.2.5.1 is met. The error ratio shall be determined after any error correction has been applied. A compliant DEV that implements the SC PHY shall achieve at least the reference sensitivity listed in Table XXX.

**Table XXX—** **Reference sensitivity levels for MCS**

|  |  |
| --- | --- |
| **MCS identifier** | **Receiver sensitivity** |
| 0 | – 66 dBm |
| 1 | – 63 dBm |
| 2 | – 59 dBm |
| 3 | – 56 dBm |
| 4 | – 52 dBm |
| 5 | – 50 dBm |
| 6 | – 44 dBm |
| 111 | reserved |

#### Receiver maximum input level

The receiver maximum input level is the maximum power level of the incoming signal, in dBm, present at the input of the receiver for which the error rate criterion in 12a.2.5.1 is met. A compliant receiver shall have a receiver maximum input level of at least –10 dBm for each of the modulation formats that the DEV supports.

### PHY layer timing

The values for the PHY layer timing parameters are defined Table XXX.

**Table XXX—PHY layer timing parameters**

|  |  |  |
| --- | --- | --- |
| **PHY parameter** | **Value** | **Subclause** |
| pPHYSIFSTime | 0.2 μs, 2.0 μs, 2.5 μs (default) | 12a.2.6.3 |
| pPHYChannelSwitchTime | 100 μs | 12a.2.6.5 |

#### Interframe space

A conformant implementation shall support the IFS parameters, as described in 8.4.1, given in Table XXX.

**Table XXX— IFS parameters**

|  |  |  |
| --- | --- | --- |
| **MAC parameter** | **Corresponding PHY parameter** | **Definition** |
| MIFS | pPHYMIFSTime | 12a.2.6.4 |
| SIFS | pPHYSIFSTime | 12a.2.6.3 |
| pBackoffslot  | pPHYSIFSTime+pCCADetectTime | 11.2.7.1 |
| RIFS | 2\*pPHYSIFSTime+pCCADetectTime | 8.4.1 |

#### Receive-to-transmit turnaround time

The receive to transmit turnaround time shall be pPHYSIFSTime, including the power-up ramp specified in 12a.2.4.3. The receive to transmit turnaround time shall be measured at the air interface from the trailing edge of the last symbol received until the first symbol of the PHY preamble is present at the air interface.

#### Transmit-to-receive turnaround-time

The transmit to receive turnaround time shall be less than pPHYSIFSTime, including the power-down ramp

specified in 12a.2.4.3.

#### Time between successive transmissions

The minimum time between successive transmissions shall be pPHYMIFSTime, including the power-up ramp specified in 12a.2.4.3. The pPHYMIFSTime shall be measured at the air interface from the trailing edge of the last symbol transmitted until the first symbol of the PHY preamble is present at the air interface.

#### Channel switch

The channel switch time is defined as the time from the last valid bit is received at the antenna on one channel until the DEV is ready to transmit or receive on a new channel. The channel switch time shall be less than pPHYChannelSwitchTime.

### PHY management for HRCP-SC PHY

The PHY PIB comprises the managed objects, attributes, actions, and notifications required to manage the HRCP-SC PHY layer of a DEV.

#### Maximum frame size

The maximum frame length allowed, pMAXFrameBodySize, shall be 1048576 octets. This total includes the MAC subheader and the MAC frame body, but not the PHY preamble, base header, (PHY header, MAC header and HCS). The maximum frame length also does not include the stuff bits.

#### Maximum transfer unit size

The maximum size data frame passed from the upper layers, pMaxTransferUnitSize, shall be 1048572 octets. If security is enabled for the data connection, the upper layers should limit data frames to 524288 octets minus the security overhead as defined in 7.3.4.2, 7.2.8.1.2, or 7.2.8.2.2.

#### Minimum fragment size

The minimum fragment size, pMinFragmentSize, allowed with the HRCP-SC PHY shall be 4096 octets.

### MIMO, channel bonding and channel aggregation

To be described in other material.

## HRCP-OOK PHY

To be described in other material.