[1]IEEE P802.15
Wireless Personal Area Networks

Project	IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)
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Re:	IEEE 802.15 TG4q
Abstract	Samsung+IMEC PHY Proposal documentation to IEEE 802.15.4q
Purpose	This document is intended to explain the overview and details of the Samsung PHY proposal submitted in response to the call for proposal (CFP) from IEEE 802.15.4q.
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Release	The contributor acknowledges and accepts that this contribution becomes the property of IEEE and may be made publicly available by P802.15.

[1] Samsung, IMEC, and * Eindhoven University of Technology

PHYSICAL LAYER PROPOSAL DOCUMENTATION

LIST OF FIGURES

LIST OF TABLES

Table of Contents

1. Introduction

The scope of this document spans the proposal for physical (PHY) layer amendment as response to the Call for Proposals issued by the IEEE 802.15.4q Task Group. This document will address the modulation, coding schemes and preambles required for the 802.15.4q physical layer. It also addresses how the proposal meets different technical requirements documented by TG4q. Finally, it summarizes the capabilities of the proposal in meeting the specifications in the technical guidance document.

2. Technical Requirements for IEEE 802.15.4q

The requirements that are set forward by the IEEE 802.15.4q are

- Support for a communication range of
  - 30 m in a free-space environment, at the lowest mandatory rate.
  - 10 m in an indoor environment, at the lowest mandatory rate.
- Ultra low power (ULP) capability of 15 mW.
- Performance requirement of 1% packet error rate (PER) for a packet size of 20 bytes.
- Regulatory compliance.

The criteria relevant to PHY layer of TG4q are

- Power consumption estimates at the transmitter and at the receiver, for an emitted isotropic radiation power (EIRP) of -5 dBm.
- Interference rejection capability.
- Co-existence with other networks.

3. Overview of Proposal

This proposal is designed to satisfy the technical requirements of the IEEE 802.15.4q. The rest of the document deals with following aspects:

- Transmission Protocol
  - Transmitter block diagram.
  - Frame format.
  - Forward error correction (FEC).
  - Interleaving.
  - Modulation based on pseudo random and orthogonal ternary sequences.
  - Pulse shaping.
  - Preamble and start frame delimiter (SFD) specifications.
  - Supported data rates.
  - Band plan and co-existence.
  - Transmit signal power spectral density.
- Receiver Architecture
  - Non-coherent receiver architecture.
- Performance Evaluation
- Link Budget Calculation
- Power Consumption
- Compliance with TGD

4. Transmission Protocol

Transmission protocol described in this section is applied to the PHY service data unit (PSDU).

4.1 Frame Format

The PHY protocol data unit (PPDU) is formed from the PSDU as shown in Figure 4.1-1.

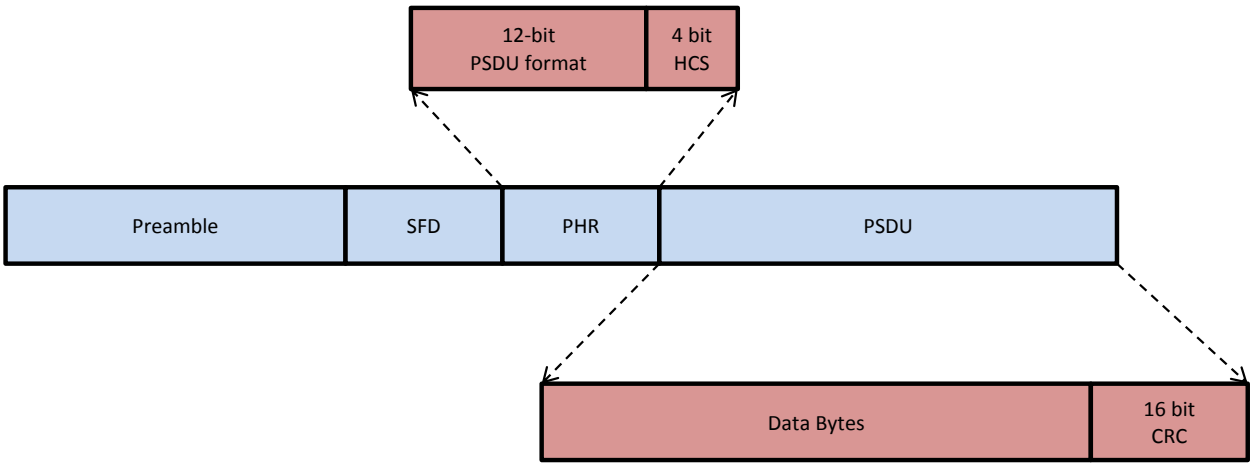

Figure 4.1-1 Physical layer frame format.

The physical layer frame consists of the following four fields:

a. Preamble: This field consists of a specific bit-pattern for frame synchronization.
b. Start frame delimiter (SFD): This field identifies the beginning of the frame and re-confirmation of the synchronization.
c. PHY Header (PHR): This field contains useful information regarding the parameters such as PSDU length indication, modulation and coding schemes used.

4.2 Transmitter Block Diagram

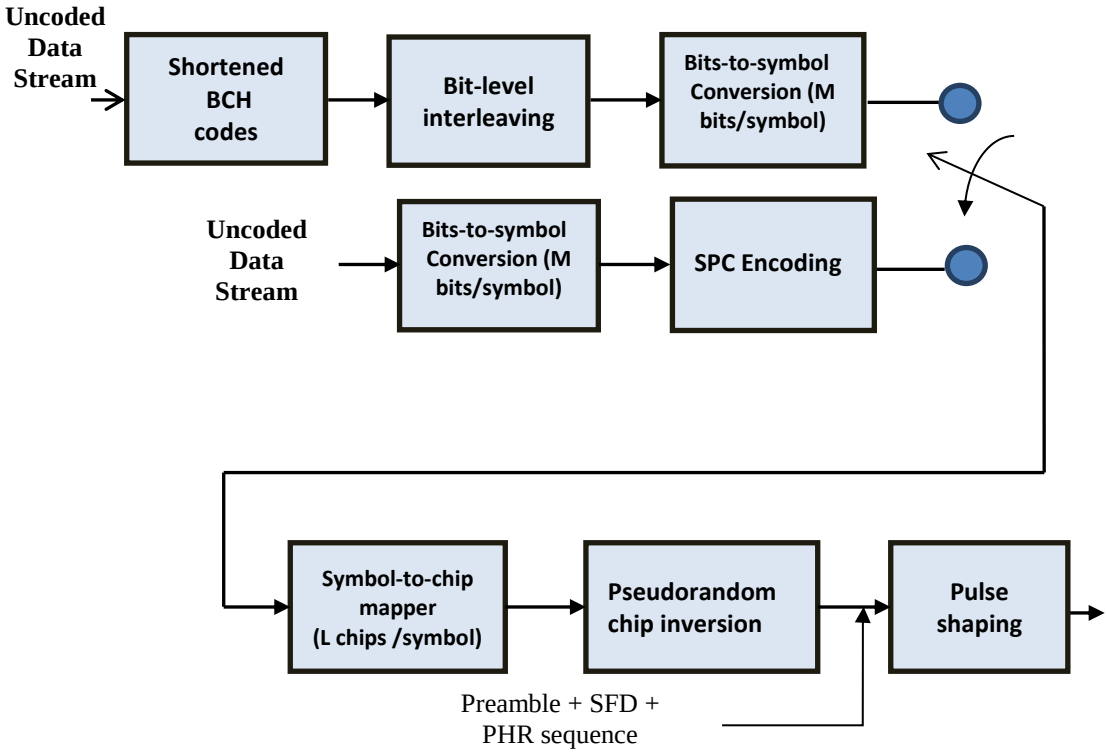

Figure 4.2-1 Block diagram of transmitter.

Uncoded data (PSDU) is received from the higher layer in form of bits, and is passed through the following baseband processing mechanisms before RF processing (up-conversion) and transmission.

1) FEC: FEC Encoding consists of either Shortened BCH encoding or Single Parity Check (SPC) encoding. Type of encoding chosen shall be indicated in physical layer header to enable the decoding in receiver. For a given packet, only one type of FEC encoding can be applied.
   - Shortened BCH encoding: to protect data against channel induced errors and to ensure uniform error protection across the data.
   - SPC encoding: to provide correction of erroneous non-binary channel symbols, wherein each channel symbol consists of M information bits.

2) Bit-level interleaving: combined with FEC to minimize bit errors in the event of symbol errors. Bit-level interleaving is applied only with BCH encoding path.
3) Bits-to-Symbol conversion: converts block of M serial bits to one symbol. This module will appear before FEC encoding in case of SPC codes and after FEC encoding and interleaving in case of BCH codes.

4) Symbol-to-chip mapping (using ternary orthogonal sequences): converts the symbol into sequence of chips, which are interpreted as channel symbols, in order to give robustness against channel noise and interference.
5) Pseudorandom chip inversion: inverts the polarity of the chips in a random fashion. This is done to minimize direct current (DC) and harmonic components in the transmitted signal, resulting in smooth continuous power spectral density (PSD). This block operates at the chip rate.
6) Pulse shaping: Performs pulse shaping to limit the out of band emissions.

In the following sections, we build a detailed framework for the transmitter blocks and their operation on incoming signals/bits.

4.3 FEC Encoding

4.3.1 Shortened BCH codes

The "Shortened BCH codes" will add error protection bits to the PSDU. The shortened versions of 2-bit error correcting BCH (63, 51) codes are used. The generator polynomial and parity polynomial for BCH (63, 51) codes are given by

$$g(x) = 1 + x^3 + x^4 + x^5 + x^8 + x^{10} + x^{12} \quad (4.3.1)$$

$$p(x) = \mathrm{mod}(x^{12}m(x), g(x)) \quad (4.3.2)$$

where m(x) is the message bits polynomial.

Parity bits for every message block can be achieved by using a simple linear feedback shift register (LFSR) circuit as shown in Figure 4.3-1.

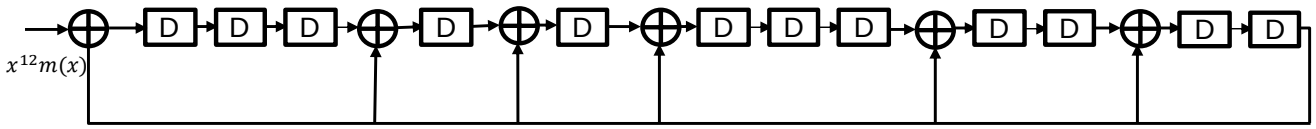

Figure 4.3-1 LFSR based implementation of parity generator for BCH (63, 51) code.

Shortened BCH codes, denoted by BCH$(63-\ell, 51-\ell)$, can be obtained from the above BCH (63,51) code for any given $1 \leq \ell < 51$. Shortened code parameters are calculated as below for any PSDU length.

Total number of message blocks

$$M_B = \left\lceil \frac{N_{PSDU}}{51} \right\rceil \quad (4.3.3)$$

N_{PSDU} – length of the packet in bits.

Length of the new message block

$$K = \left\lceil \frac{N_{PSDU}}{M_B} \right\rceil \quad (4.3.4)$$

Shortening length of the code

$$\ell = 51 - K \quad (4.3.5)$$

Length of the new encoded block

$$N = 63 - \ell \quad (4.3.6)$$

Length of the new bit-stream

$$N_{zeropad} = M_B\, K \quad (4.3.7)$$

Required number of zeros for insertion

$$Z = N_{zeropad} - N_{PSDU} \quad (4.3.8)$$

Thus, M_B message blocks of K bits are formed. Each of these message blocks is passed through the parity generator circuit (shown in Figure 4.3-1) to yield the corresponding 12-bit parity. The resulting parity bits are appended at the end of the message block to obtain the corresponding codeword. The total number of bits at the output of shortened BCH codes block for a PSDU can be calculated as

$$N_{coded} = M_B N \quad (4.3.9)$$

4.3.2 SPC code

SPC codes add an error correction symbol to the transmitted channel symbols. A $(9,8)_q$ SPC code is used to protect every 8 channel symbols, where $q = 2^M$. The value of M is determined by the bits-to symbol conversion stage. The parity-check symbol is generated such that the summation of 9 channel symbols (including the parity-check symbol) is constrained to 0 over $GF(q)$. By representing each M-bit tuple as an element in $GF(q)$ which is denoted by $\widetilde{w}_n$, the parity symbol generation is simply given by

$$\widetilde{w}_9 = \sum_{n=1}^{8} \widetilde{w}_n$$

where the summation is taken over $GF(q)$. The parity-check symbol can be generated by using a circuit working over $GF(q)$ as shown in Figure 4.3-2.

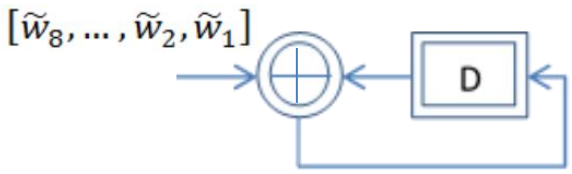

Figure. 4.3-2 Implementation of parity-check symbol generator for $(9,8)_q$ SPC code.

Once M is fixed, the code parameters are calculated as below for any PSDU length.
Total number of message blocks

$$M_B = \left\lceil \frac{N_{PSDU}}{8M} \right\rceil$$

For the last message block, Z zero bits are padded where

$$Z = 8MM_B - N_{PSDU} \ .$$

4.4 Bit-level Interleaving

Once codewords are obtained from the BCH encoder, bit-level interleaving is performed on the encoded data, where bits across codewords are interleaved with an appropriate chosen depth. The primary purpose of this operation is to protect bit errors against symbol errors. Typically, the interleaving depth is chosen based on the modulation. Let N be the length of the codeword. Let d be the interleaver depth. The following procedure is followed for one round of interleaving:

a. Collect d blocks of codewords
b. Write them **row-wise** in a $d \times N$ dimensional array.
c. Read the array **column-wise** and output the data sequentially.

The following sketch depicts the procedure for an interleaving depth of $d = 4$.

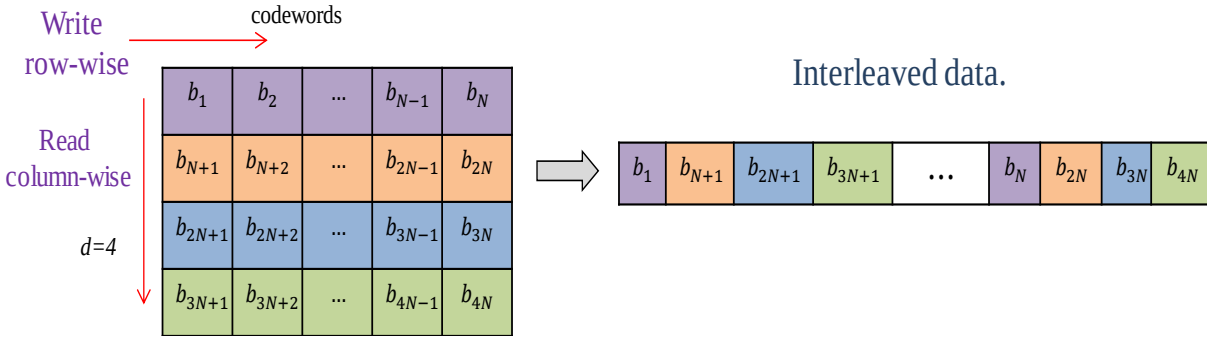

Figure 4.4-1 Interleaving operation for depth d = 4.

4.4.1 Calculation of interleaving blocks

Next, we outline the calculation of number of interleaving blocks and interleaving depth for each block shown in Table 4.4-1. Let M_B be the number of codewords obtained from

the encoder stage. Depending on the modulation size of M, choose initial interleaver depth d as M as shown in Table 4.10-1 Preamble, SFD/PHR, modulation combinations and corresponding data rates based on using (63,51) BCH code.

Obtain the residual interleaver depth,

$$d_R = mod(M_B, d) \quad \textbf{(4.4.1)}$$

Number of interleaving blocks,

$$N_B = \lceil M_B / d \rceil \quad (\mathbf{4.4.2})$$

Maximum interleaving depth,

$$d_{\max} = 5. \quad \textbf{(4.4.3)}$$

Table 4.4-1 Calculation of interleaving depth.

Condition			**Interleaving depth**
$d_R = 0$			Apply depth 'd' interleaving for N_B blocks
$d_R \neq 0$	$M_B < d$		Apply depth 'd_R' interleaving for N_B blocks
	$M_B > d$	$d+d_R \leq d_{\max}$	Apply depth 'd' interleaving for the first (N_B-2) blocks, '$d+d_R$' interleaving for the last one block
		$d+d_R > d_{\max}$	Apply depth 'd' interleaving for the first (N_B-2) blocks, and apply depth $\lceil (d+d_R)/2 \rceil$ for the (N_B-1)th block, depth $\lfloor (d+d_R)/2 \rfloor$ for the N_B^{th} block

4.5 Bits-to-Symbol Conversion

This block takes the bit stream from the interleaver, and packs them into blocks of M bits each. Each block comprises a "symbol". Therefore, we can interpret this as each symbol conveying M bits of information. After packing, each symbol is passed to the modulation block for symbol-to-chip mapping. The value of M is chosen appropriately based on the modulation scheme employed.

4.6 Modulation: Symbol-to-Chip Mapping

This part performs the baseband modulation. In the present context, the modulation is performed by a process of mapping symbol to a sequence of chips. Succinctly, for every symbol (M bits/symbol) generated at its input, the modulator outputs a unique sequence from a pre-defined set of L-length ternary sequences. The ratio $SF = L/M$ is the spreading factor of the modulation scheme. The choice of SF is determined by the data rate requirements. We call this as the ***Variable Spreading Factor-Ternary ON-OFF Keying*** (VSF-TOOK).

The "Bits-to-Symbol Converter"- stage converts binary stream of bits into a sequence of M-bit symbols. Equivalently, this procedure maps bit stream from binary alphabet on to a symbol alphabet $\mathbb{S}$, which is defined as

$$\mathbb{S} \stackrel{\text{def}}{=} \{0, 1, \ldots, A-1\}, \qquad \text{where } A = 2^M.$$

Corresponding to each symbol $m \in \mathbb{S}$, define a unique L-length, ternary sequence as

$$\mathbf{c}_m = \left[c_m[0], \ldots, c_m[L-1]\right]^T, \qquad c_m[n] \in \{-1, 0, +1\} \;\; n \in \{0, \ldots, L-1\}.$$

The collection of these sequences is denoted by the set

$$\mathbb{C} \stackrel{\text{def}}{=} \{\mathbf{c}_0, \ldots, \mathbf{c}_{A-1}\}.$$

We call the set $\mathbb{C}$ as the *spreading code* and its elements are called the *spreading sequences.* It needs to be emphasized that the spreading code $\mathbb{C}$ is designed such that the spreading sequences in the set are mutually near-orthogonal, i.e., ideally it is expected that $\mathbf{c}_{m_1}^{\mathrm{T}}\mathbf{c}_{m_2} = 0, \; \forall\, \mathbf{c}_{m_1}, \mathbf{c}_{m_2} \in \mathbb{C}, \; m_1 \neq m_2$.
We define the modulation using spreading sequences as the mapping:

$$\mathcal{M}: \mathbb{S} \rightarrow \mathbb{C}.$$

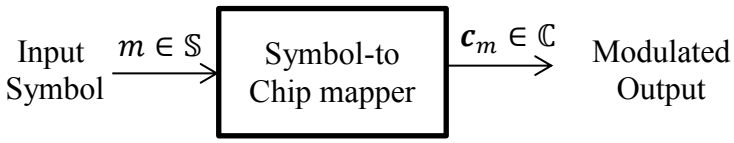

Figure 4.6-1 Modulation process: Symbol-to-chip mapping.

For the given symbol m, in a pre-determined manner, the modulator maps it onto a specific spreading sequence $\mathbf{c}_m$ in $\mathbb{C}$. This procedure is illustrated in Figure 4.6-1.

4.6.1 Design of spreading codes

There are two types of codes chosen for modulation: orthogonal codes and pseudorandom codes.

i. **Orthogonal code:** This code consists of a set of mutually orthogonal sequences, to map the source alphabet. Therefore, to represent a symbol from the set of $A = 2^M$ -ary alphabet, an orthogonal code will have a set of A orthogonal sequences.

ii. **Pseudorandom code:** This code consists of a set of $A = 2^M$ sequences with good cross-correlation properties. The sequences are typically chosen to be pseudorandom sequences. To reduce the complexity of implementation, we can generate the pseudorandom code as follows:

   a) Obtain an L-length pseudorandom sequence with good cyclic autocorrelation property. This is the spreading sequence $\mathbf{c}_0$. We call this the *"basic sequence".*

   b) For $m = 1, \ldots, A-1$, right circular-shift $\mathbf{c}_0$ by m positions to obtain $\mathbf{c}_m$, $m = 1, \ldots, A-1$.

   The above procedure generates the spreading code $\mathbb{C} = [\mathbf{c}_0, \cdots, \boldsymbol{c}_{A-1}]$ **.** Since we start with the basic sequence $\mathbf{c}_0$ that has good cyclic autocorrelation properties, it is guaranteed that elements of $\mathbb{C}$ exhibit good cross-correlation properties.

4.6.2 Definitions of modulation schemes

The choice of modulation schemes depends on the factors such as the performance and required data rate. The following tables give the different modulation schemes employed, with their definitions and the nomenclature.

Table 4.6-1 Orthogonal codes.

M	L	Nomenclature	Orthogonal Sequences
1	1	1/1-TOOK	[0; 1]
2	4	2/4-TOOK	[1 0 0 0; 0 1 0 0; 0 0 1 0; 0 0 0 1]

Table 4.6-2 Pseudorandom codes.

M	L	Nomenclature	Basic Sequence ($\mathbf{c_0}$)
3	8	3/8-TOOK	[0 0 0 1 -1 0 1 1]
5	32	5/32-TOOK	[-1 0 0 1 0 1 -1 0 -1 -1 1 -1 0 1 0 1 0 0 0 1 0 0 1 1 -1 0 0 0 0 0 1 1]

Table 4.6-3 Illustrative example for modulation for *M* = 1.

Bits b_0	Symbol Alphabet $\mathbb{S}$	Spreading Code $\mathbb{C}$
0	0	[0]
1	1	[1]

Table 4.6-4 Illustrative example for modulation for *M* = 2.

Bits $b_0 b_1$	Symbol Alphabet $\mathbb{S}$	Spreading Code $\mathbb{C}$
00	0	[1 0 0 0]
10	1	[0 1 0 0]
11	2	[0 0 1 0]
01	3	[0 0 0 1]

Table 4.6-5 Illustrative example for modulation for *M* = 3.

Bits $b_0 b_1 b_2$	Symbol Alphabet $\mathbb{S}$	Spreading Code $\mathbb{C}$
000	0	$\mathbf{c}_0$
100	1	$\mathbf{c}_1$
110	2	$\mathbf{c}_2$
010	3	$\mathbf{c}_3$
011	4	$\mathbf{c}_4$
111	5	$\mathbf{c}_5$
101	6	$\mathbf{c}_6$
001	7	$\mathbf{c}_7$

Table 4.6-6 Illustrative example for modulation for M = 5.

Bits $b_0b_1b_2b_3b_4$	Symbol Alphabet $\mathbb{S}$	Spreading Code $\mathbb{C}$
00000	0	$\mathbf{c}_0$
10000	1	$\mathbf{c}_1$
11000	2	$\mathbf{c}_2$
01000	3	$\mathbf{c}_3$
01100	4	$\mathbf{c}_4$
11100	5	$\mathbf{c}_5$
10100	6	$\mathbf{c}_6$
00100	7	$\mathbf{c}_7$
00110	8	$\mathbf{c}_8$
10110	9	$\mathbf{c}_9$
11110	10	$\mathbf{c}_{10}$
01110	11	$\mathbf{c}_{11}$
01010	12	$\mathbf{c}_{12}$
11010	13	$\mathbf{c}_{13}$
10010	14	$\mathbf{c}_{14}$
00010	15	$\mathbf{c}_{15}$
00011	16	$\mathbf{c}_{16}$
10011	17	$\mathbf{c}_{17}$
11011	18	$\mathbf{c}_{18}$
01011	19	$\mathbf{c}_{19}$
01111	20	$\mathbf{c}_{20}$
11111	21	$\mathbf{c}_{21}$
10111	22	$\mathbf{c}_{22}$
00111	23	$\mathbf{c}_{23}$
00101	24	$\mathbf{c}_{24}$
10101	25	$\mathbf{c}_{25}$
11101	26	$\mathbf{c}_{26}$
01101	27	$\mathbf{c}_{27}$
01001	28	$\mathbf{c}_{28}$
11001	29	$\mathbf{c}_{29}$
10001	30	$\mathbf{c}_{30}$
00001	31	$\mathbf{c}_{31}$

4.7 Pseudorandom Chip Inversion

This block is used to remove the DC component and mitigate the spectral lines in the transmitted signal. This is achieved by inverting the polarity of each chip in a pseudorandom manner. Thus, it eliminates the dependence of a signal's spectrum upon the actual transmitted data, making it more dispersed to meet the spectral regulation requirements. This operation works at the chip level and the random phase inversion is achieved by the use of a pseudorandom binary sequence (PRBS) generator, whose output is used in deciding whether to invert the spreading sequence or not. The sketch of the block is shown in Figure 4.7-1.

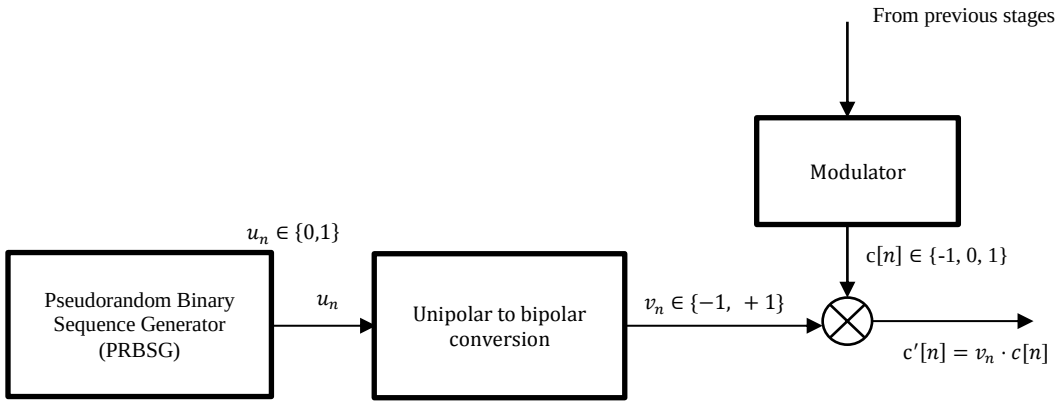

Figure 4.7-1 Schematic of the pseudorandom chip inversion stage.

The PRBS generator is obtained by using the ITU 16-bit scrambler. The shift register implementation of PRBS generator is illustrated in Figure 4.7-2

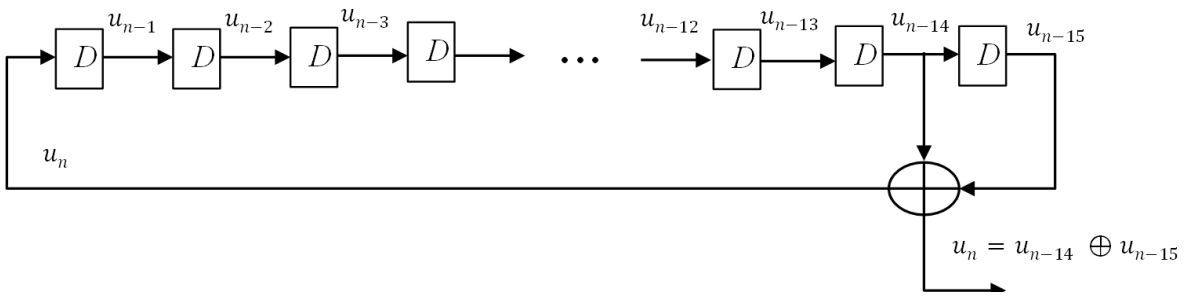

Figure 4.7-2 Linear feedback shift register based implementation of the PRBS generator.

The PRBS generator employs the generator polynomial

$$G(x) = 1 + x^{14} + x^{15}.$$

Therefore, the pseudorandom binary sequence output is generated recursively as

$$u_n = u_{n-14} \oplus u_{n-15}, \qquad n = 0, 1, 2, \ldots$$

where $\oplus$ is the modulo-2 addition operator. Further, the initial seed of the PRBS is denoted by

$$u_{init} = [u_{-1}, \ \ldots, u_{-14}, \ u_{-15}].$$

Default value of u_{init} i is 0x5B47.The randomization pattern of chip inversion depends on u_{init}.

The output of the PRBS generator $\{u_n\}$, which is a unipolar binary sequence, is passed through the bipolar converter to yield a bipolar sequence $\{v_n\}$. The conversion operation can be represented as

$$v_n = 2u_n - 1.$$

That is

$$v_n = \begin{cases} 1 & \text{if } u_n = 1 \\ -1 & \text{if } u_n = 0 \end{cases}.$$

The polarities of the chips are randomly inverted as

$$c'[n] = v_n \cdot c[n], \qquad c[n] \in \{-1, 0, 1\}, \quad n = 0, 1, 2, \ldots$$

4.8 Pulse Shaping

The Gaussian pulse with a time-bandwidth product of BT = 0.3 is used as the pulse shaping filter. The impulse response of the filter is given by

$$g(t) = B\sqrt{2\frac{\pi}{\ell n(2)}} * e^{-\left(\frac{2\pi^2 B^2 t^2}{\ell n\, 2}\right)} \qquad (4.8.1)$$

where B is the bandwidth. The time domain response and frequency domain response of the Gaussian pulse shaping filter with BT = 0.3 and $T = 1\ \mu s$ are as illustrated below

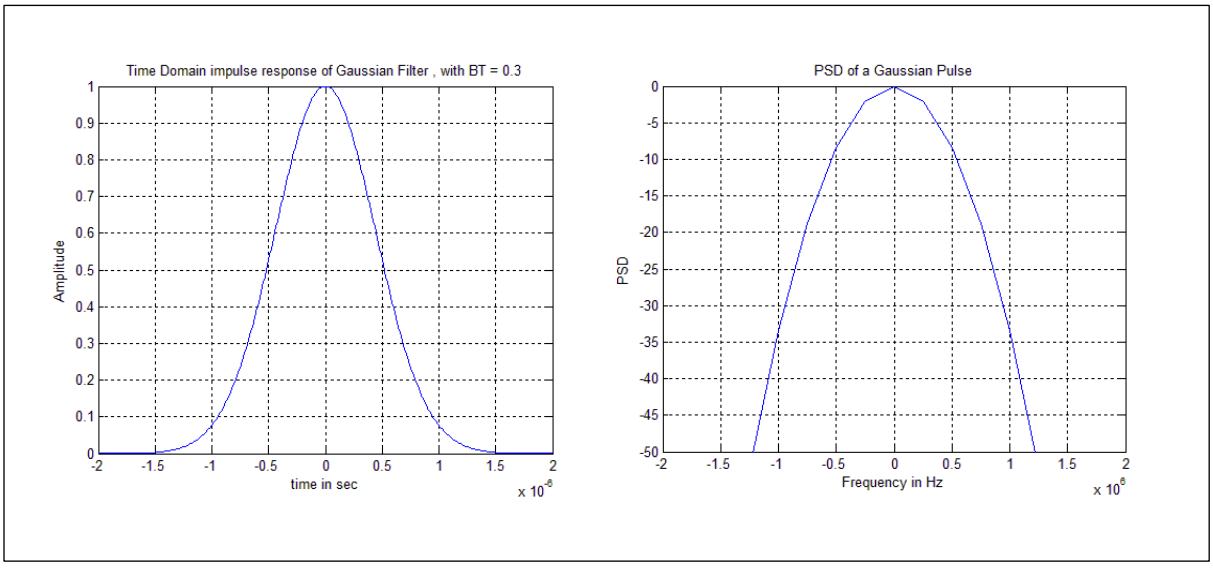

Figure 4.8-1 Time domain and frequency domain responses of the Gaussian pulse shaping filter.

4.9 Preamble and SFD/PHR

Two different preambles are defined for supporting multiple data rates in order to maximize the energy efficiency of PSDU. For any preamble, a 32-chip sequence is repeated N_{rep} times. Preamble is immediately followed by an SFD bit-pattern which is again spread by a spreading sequence given in Table 4.9-2. Depending on the length and type of spreading sequence used, two different combinations of preamble and SFD/PHR are defined.

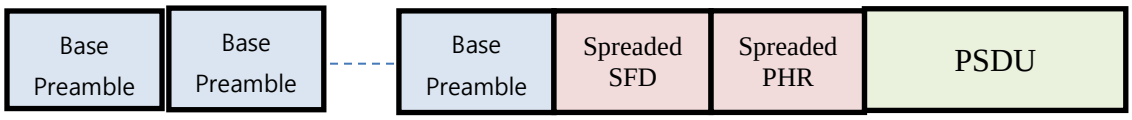

Figure 4.9-1 Preamble and SFD/PHR structure.

The values for base preamble and N_{rep} are given below in Table 4.9-1.

Table 4.9-1 Definitions related to ternary preamble sequences.

Preamble Format	Spreading Factor (SF)	Number of Repetitions (N_{rep})	Base Preamble Sequence
P2	4	4	[1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 -1 -1 0 0 1 -1 0 0 1 -1 0 0 1 -1 0 0 -1]
P3	8	8	[1 0 -1 0 0 -1 0 -1 1 0 1 0 0 -1 0 1 1 0 1 0 0 -1 0 1 -1 0 1 0 0 1 0 1]

Final sequence of spreaded SFD/PHR is obtained by spreading the 8 bit base sequence [0 1 0 1 1 0 0 1] by a spreading sequence. The spreading sequences for different SFD/PHR are given in Table 4.9-2. These spreading sequences are referred as S2 and S3.

Table 4.9-2 Spreading sequences for SFD/PHR.

Spreading Format	Spreading Factor (SF)	Spreading sequence for SFD/PHR (for bit 1 and bit 0)
S2	4	1 → [1 0 0 1] 0 → [0 -1 -1 0]
S3	8	1 → [1 0 -1 0 0 -1 0 1] 0 → [0 -1 0 1 1 0 -1 0]

PHY Header (PHR) field contains useful information regarding the PSDU format such as length indication, modulation and coding schemes used. The modulation used for PHY header is same as that used for modulation of Start Frame Delimiter (SFD) given in Table 4.9-2.

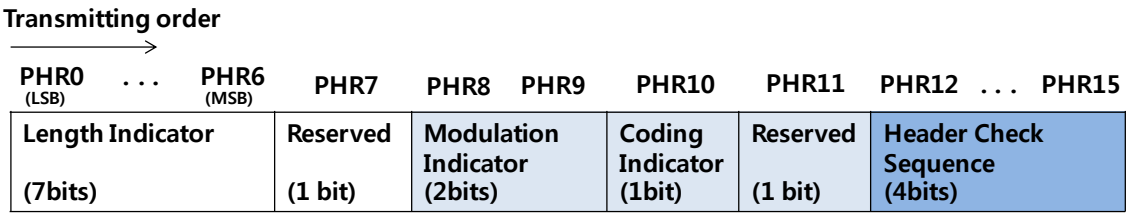

Figure 4.9-2 PHY header description.

Table 4.9-3 Modulation indicator for PSDU.

{PHR9, PHR8}	Modulation
{0, 0}	1/1-TOOK
{0, 1}	2/4-TOOK
{1, 0}	3/8-TOOK
{1, 1}	5/32-TOOK

Table 4.9-4 Coding indicator for PSDU.

{PHR10}	Coding
{0}	BCH
{1}	SPC

The Length Indicator (LI) is a 7 bit field which is used for length indication ranging from 0 to 127 bytes with LSB as first bit in transmission order. The Modulation Indicator is 2 bit field to indicate the modulation scheme of PSDU as shown in Table 4.9-3. The Coding Indicator is 1 bit field to indicate the coding scheme of PSDU as shown in Table 4.9-4. Combinations of Modulation Indicator and Coding Indicator are referred as Transmission Format Indicator (TFI) to indicate Modulation and Coding Scheme (MCS) of PSDU immediately followed by PHR. The HCS is obtained by taking 2's complement of the reminder of PHY header bits with generator polynomial given as

$$g(x) = 1 + x + x^4$$

4.10 Data Rates Supported

The data rates supported for 2.4 GHz and 900 MHz are listed in **Error! Reference ource not found.**. The chip rate considered for 2.4 GHz and 900 MHz bands are 1 Mcps

and 600 Kcps respectively. The Preamble and SFD to be used for these data rates are mentioned as well in the **Error! Reference source not found.**.

Table 4.10-1 Preamble, SFD/PHR, modulation combinations and corresponding data rates based on using (63,51) BCH code.

PSDU Format	Modulation Format	Modul-ation Duty Cycle	Initial Inter-leaver depth (d)	M (bits per Symb)	L (chips Per Symb)	Data Rate in 2.4 GHz (kbps)	Data Rate in 900 MHz (kbps)	Preamble Format	SFD/PHR Spreading Format
D1	1/1-TOOK	0.50	1	1	1	809.5	485.7	P3	S3
D2	2/4-TOOK	0.25	2	2	4	404.8	242.8	P3	S3
D3	3/8-TOOK	0.50	3	3	8	303.5	182.14	P3	S3
D6	5/32-TOOK	0.50	5	5	32	126.5	75.9	P3	S3

Table 4.10-2 Payload efficiencies for a payload size of 40 bytes.

Data Rate Number	D1	D2	D3	D6
Payload efficiency for 40 bytes (%)	63.83	77.92	70.18	84.96

Table 4.10-3 Preamble, SFD/PHR, modulation combinations and corresponding data rates based on using (9,8) SPC code.

PSDU Format	Modulation Format	Modul-ation Duty Cycle	M (bits per Symb)	L (chips Per Symb)	Data Rate in 2.4 GHz (kbps)	Data Rate in 900 MHz (kbps)	Preamble Format	SFD/PHR Spreading Format
D8	1/1-TOOK	0.50	1	1	889	533.33	P2	S2
D9	2/4-TOOK	0.25	2	4	444.5	266.66	P2	S2

4.11 Band Plan and Co-existence

The band plan proposal is exactly similar to that of **IEEE 802.15.4 2011** document to enable the co-existence with existing IEEE 802.15.4 physical layers and other standards. The band plans for 2.4 GHz and 900 MHz bands are as shown below.

For 2.4 GHz Band:

$$F_c = 2405 + 5k\,, \qquad k = 0,1,\ldots,15. \qquad (4.11.1)$$

For 900 MHz Band:

$$F_c = 906 + 2k\,, \qquad k = 0,1,\ldots,9. \qquad (4.11.2)$$

4.12 Power Spectral Density

The power spectral density of the modulated baseband signal for 1 Mcps chip rate is as shown in Figure 4.12-1.

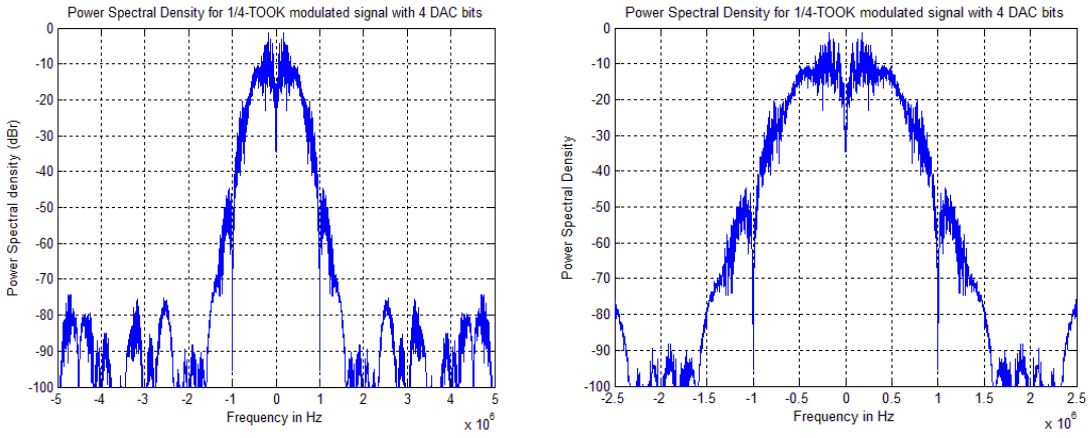

Figure 4.12-1 Power spectral density for modulated waveform with resolution of 4-bit DAC.

Table 4.12-1 Adjacent and Alternate channel leakage ratios.

POWER LEAKAGE RATIO	VALUE
Adjacent channel leakage ratio	-69 dB
Alternate channel leakage ratio	-72 dB

5 Receiver Architecture

The transmission protocol proposed allows both the coherent and non-coherent form of reception. However, in this article, unless mentioned, the architecture and the results presented hold for non-coherent receiver. For benchmarking, results for ideal coherent receiver are also published.

5.1 Receiver Block Diagram

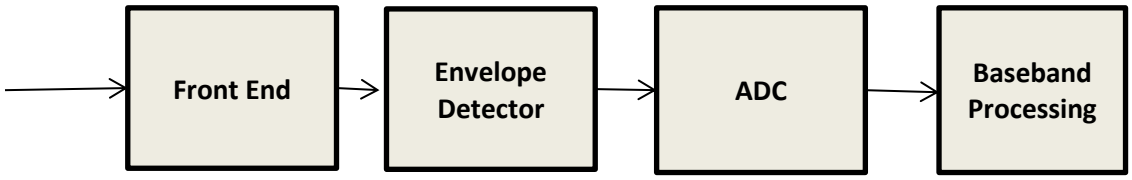

Figure 5.1-1 Non-coherent receiver architecture.

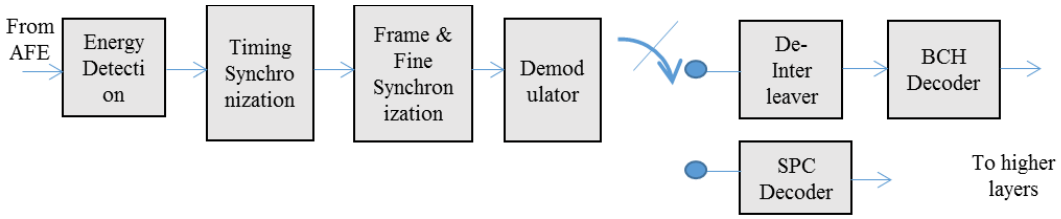

Figure 5.1-2 Block diagram of baseband processing at the receiver.

The receiver front-end used for the non-coherent reception of data is based on the super-regenerative principle.

5.1.1 Energy detection

Energy detector detects the presence of useful signal. This is performed by accumulating signal energy of 16 chips and then comparing it against a pre-computed threshold.

$$signal\ present = \begin{cases} 1 & if \sum_{n=1}^{16} y(n)^2 \geq \gamma_{TH} \\ 0 & otherwise \end{cases} \qquad (5.1.1)$$

5.1.2 Timing synchronization

Timing synchronization is performed by sliding correlation of input signal in unipolar mode with preamble template in bi-polar mode. Length of each correlation window is N_p chips. The time at which the maximum correlation is achieved is taken as symbol timing estimate, $\hat{\tau}$, given by

$$\hat{\tau} = \underset{j}{\text{argmax}} \sum_{i=1}^{N_p} x[i]y[i+j] \qquad (5.1.2)$$

$\left[x[1], x[2] \ldots, x\left[N_p\right]\right]$ – Preamble template at Rx

$\{y[1], y[2] \ldots, \}$ – baseband samples at Rx

5.1.3 Frame synchronization

Once timing synchronization is obtained through preamble, SFD is used for the re-confirmation of the timing estimate. This is achieved by decoding the SFD field bit-by-bit, and then comparing the resultant bit-pattern with the actual SFD bit-pattern.

5.1.4 Demodulator

The demodulator detects the transmitted symbol based on correlation of spreading sequences. The demodulator calculates the correlation metric of the received chip sequence with all possible chip sequences to obtain hard decision of the channel symbol. The transmitted symbol is detected as the symbol corresponding to the chip sequence which gives the maximum correlation.

Symbol estimate at epoch n, $\hat{m}_n$

$$\widehat{m}_n = \underset{m\in\{0,\ldots,\, A-1\}}{\operatorname{argmax}} \mathbf{s}_m^T \mathbf{y}_n$$

$y_n^T = [y_n[1], \ldots, y_n[L]]$ – received samples corresponding to symbol at epoch *n*
$\mathbf{s}_m^T = \left[s_m[1], \ldots, s_m[L]\right]$ – spreading sequence corresponding to the symbol *m*.

For SPC decoding, reliability measures (likelihoods) need to be estimated. At epoch n, received samples of corresponding received symbol are stored in $\boldsymbol{y}_n = [y_n[1], \ldots, y_n[L]]$. The reliability vector $\boldsymbol{r}_n$ is calculated as

$$\boldsymbol{r}_n = \boldsymbol{S}^T \boldsymbol{y}_n$$

where $\boldsymbol{S} = [\boldsymbol{s}_0, \boldsymbol{s}_1, \ldots, \boldsymbol{s}_{A-1}]$ and $\boldsymbol{r}_n = \left[r_n[1], \ldots, r_n[L]\right]$. Here $r_n[m]$ represents the reliability measure for receiving symbol m at epoch n. For the case where $A = L = 1$, $\boldsymbol{S} = 1$. We emphasize that for 1/1-TOOK, we use threshold-based detection where the optimal threshold shall be estimated with the preamble sequence.

5.1.5 De-Interleaver

This block performs the inverse operation of interleaver described in the transmitter section 4.4, and recovers the encoded bits from interleaved data.
The following procedure is followed for one round of de-interleaving:

a. Collect $d \cdot N_{new}$bits.
b. Write them **column-wise** in a $d \times N_{new}$ dimensional array.
c. Read the array **row-wise** and output the data sequentially.

5.1.6 BCH decoder

The BCH decoder recovers the message bits from the received codewords. During the process of decoding, the decoder corrects bit-errors induced by the channel. We employ a BCH$(63 - \ell, 51 - \ell)$ decoder which can correct up to 2 bit errors per codeword. More details on decoding process and algorithms can be found in classical texts such as [1].

5.1.7 SPC decoder

The SPC decoder recovers the message symbols from the received codeword. A Wagner-like decoding can be employed to correct up to one channel symbol. More details on decoding of a non-binary SPC code is can be found in [2].

6 Performance Curves

This section describes the performance of the proposed system for various proposed modulation formats under various channel conditions.

6.1 Performance in AWGN Channel with SRR RF Impairments

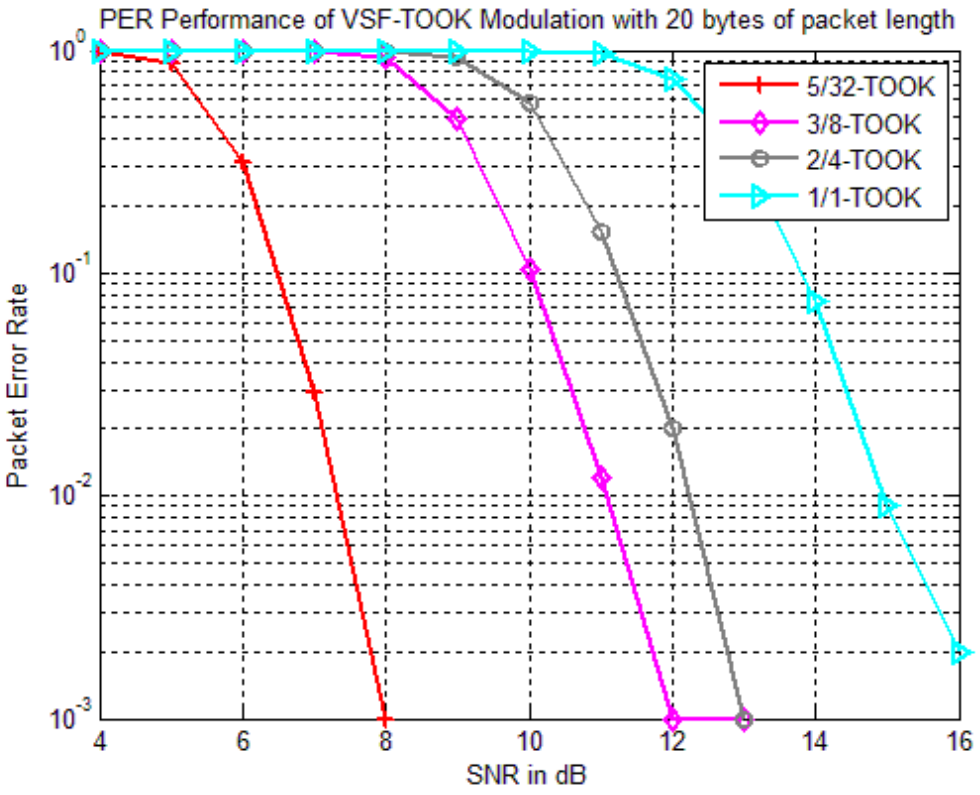

Figure 6.1-1 Packet error rate (PER) vs. SNR curves under AWGN for the non-coherent reception.

Table 6.1-1 List of required SNRs for different modulations to meet a target PER of 1%.

Modulation Scheme	SNR (dB) @ PER=1%.
1/1-TOOK	15
2/4-TOOK	12.25
3/8-TOOK	11
5/32-TOOK	7.25

6.2 Performance in AWGN with Interference for SRR

We evaluated the performance of our system in presence of homogenous interference. The two standard cases are considered. First one is the adjacent channel interference (ACI), where the interference is due to the transmissions from the adjacent channel, i.e., the channel spaced 5 MHz apart from the operating center frequency. Second scenario is the alternate channel interference (ALCI) where the interference is due to the transmissions from the alternate channel, i.e., channels spaced 10 MHz apart from the operating center frequency. For simulation purposes, the interference patterns were generated by simulating the transmitter using pseudorandom message bits. The performance evaluation considers the combined performance of both synchronization as well as demodulation blocks. The following plots show the performance of various modulation schemes in different interference scenarios.

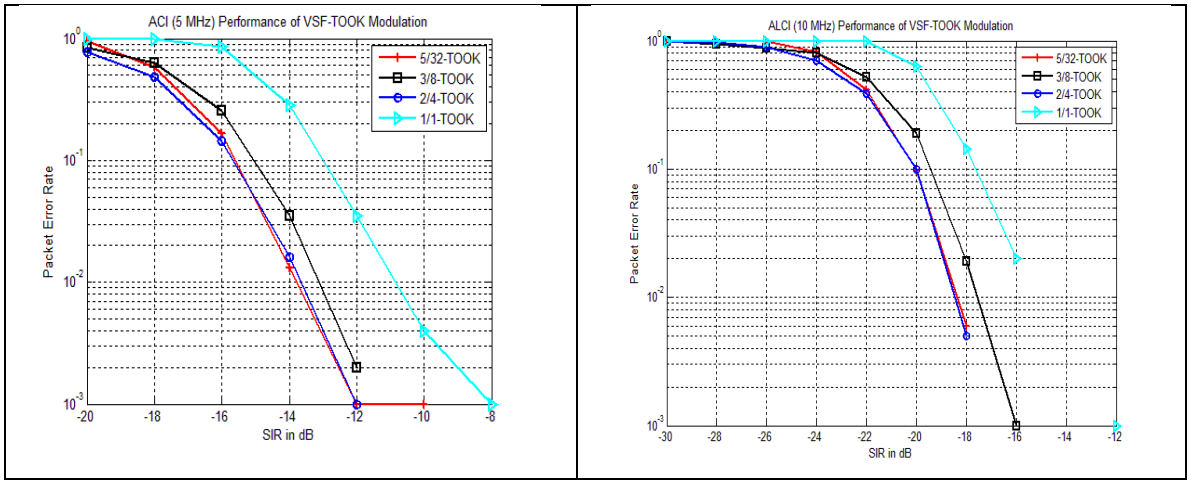

Figure 6.2-1 Interference rejection results for proposed modulation schemes.

Table 6.2-1 Out-of-Band interference rejection capability.

Interference Rejection	Value (dB)
Adjacent Channel Rejection	13
Alternate Channel Rejection	20

6.3 Synchronization Performance of the Preambles

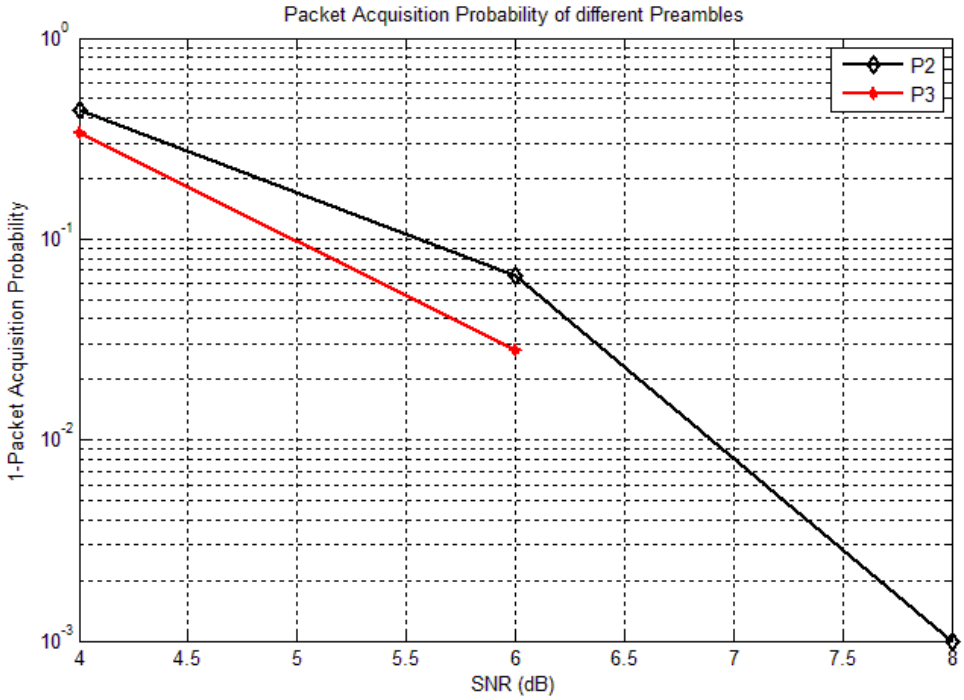

Figure 6.3-1 Misdetection plots for proposed preamble.

6.4 Performance Curves for AWGN Channel without RF Impairments

The packet error performance of the proposed modulation schemes in AWGN channel with no RF impairments is given in this section. The results are given for coherent and non-coherent receivers. In addition, we have also given the synchronization mis-detection for proposed preambles.

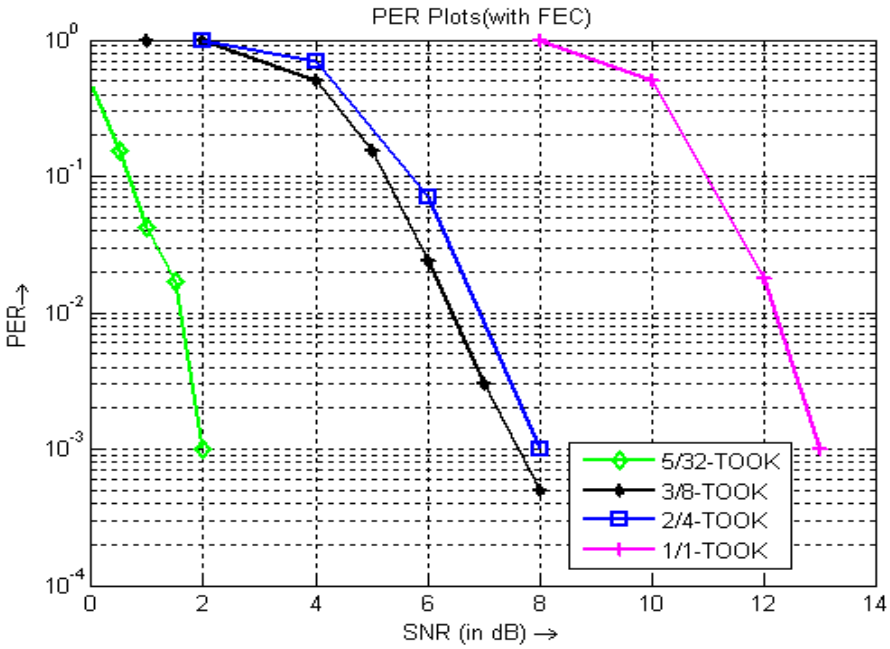

Figure 6.4-1 Packet error rate for proposed modulation schemes with BCH encoding.

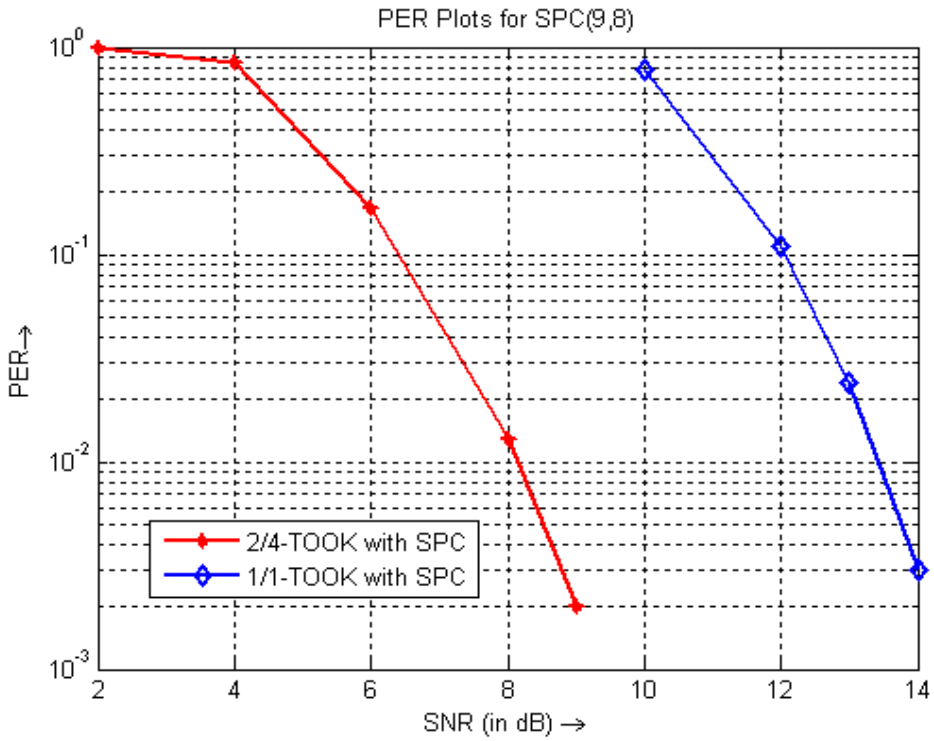

Figure 6.4-2 Packet error rate for proposed modulation schemes with SPC encoding.

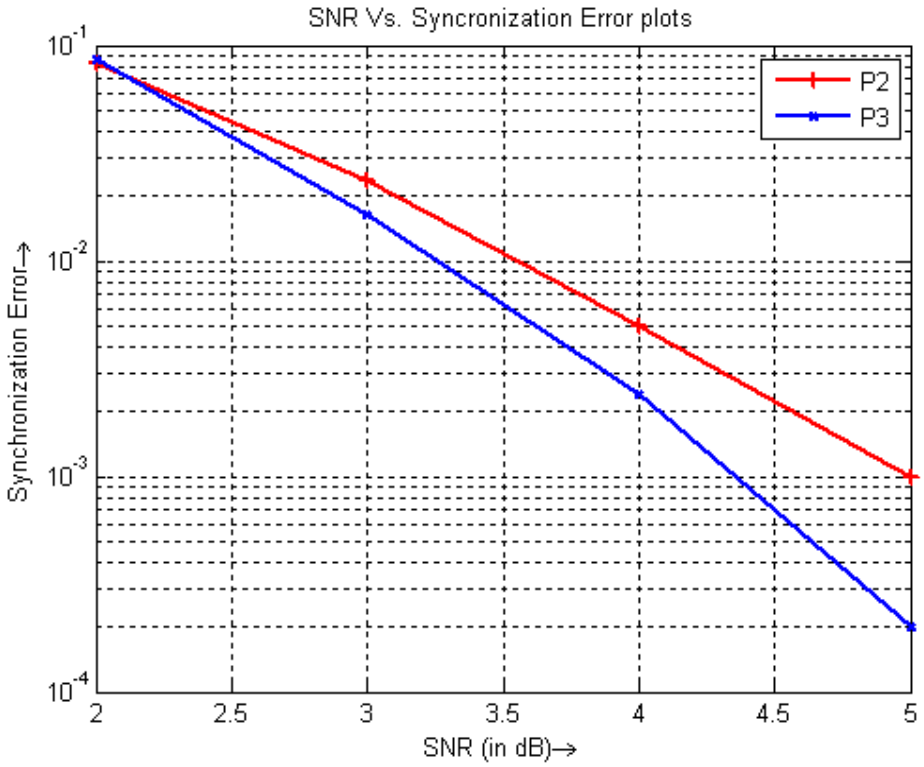

Figure 6.4-3 Packet acquisition probability vs. SNR curves for proposed preambles.

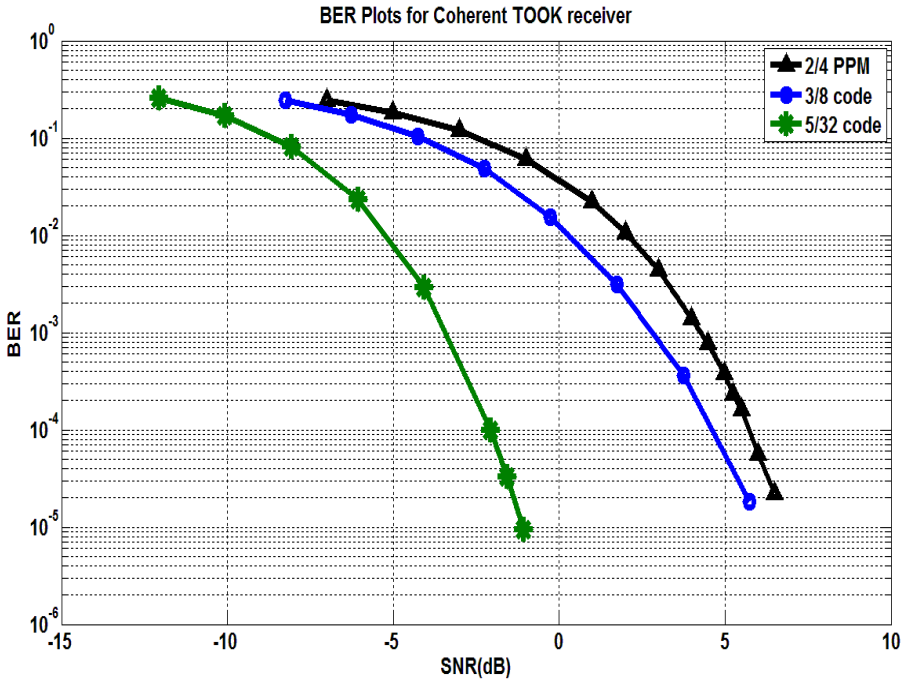

Figure 6.4-4 Bit error rate for proposed modulation schemes with coherent receiver.

7 Link Budget Calculations

We present link-budget calculations for free-space and indoor environments. The data rates considered here are the ones with BCH encoding.

7.1 Link Budget for Indoor Path Loss Environment

Table 7.1-1 Link budget for AWGN channel.

Parameter	**D6 (5/32-TOOK)**	**D1 (1-TOOK)**
Payload Data Rate (R_b) in kbps	126.48	809.50
Distance (d) in m	30.00	30.00
Bandwidth (B) in MHz	1.00	1.00
Tx Antenna Gain (G_T) in dB	0.00	0.00
Center Frequency (F_C) in MHz	2450.00	2450.00
Average Transmit Power (P_t) in dBm	-5.00	-5.00
Path Loss at distance d m in dBm	69.77	69.77
Rx Antenna Gain (G_R) in dB	0.00	0.00
Received Power (P_{rx}) in dBm	-74.77	-74.77
Average Noise Power Per bit (N) in dBm	-122.98	-114.92
System Noise Figure (NF) in dB	10.00	10.00
Minimum EbNo Required in dB	9.56	12.50
Implementation Loss (I) in dB	3.00	3.00
Link Margin (LI) in dB	**25.65**	**14.65**
Receiver Sensitivity (S) in dBm	**-100.42**	**-89.42**

8 Power Consumption Table

The power consumption of the transmitter at -5 dBm EIRP is around 5 mW. The power consumption of the receiver is less than 4 mW and is measured at 3 dB above receiver sensitivity. The power consumption is measured both at the transmitter and at the receiver with a packet size of 20 bytes

8.1 Power Consumption for SRR

Table 8.1-1 Power consumption figures for the non-coherent transceiver architecture.

Tx Component	Power (µW) @ -5 dBm
Baseband	1000
VCO	322
Power Amplifier	2982
PLL + Freq Synthesizer	1000
Total	5304

Rx Component	Power (µW)
LNA+SRO	638
ED+VGA	33
ADC (8 bit)	7.5
Baseband	1500
PLL + Freq Synthesizer	1000
Total	3178.5

9 Summary

Samsung and IMEC merged PHY proposal to IEEE 802.15.4q amendment is presented in this document. The transmission protocol, receiver architecture and performance results for the proposed modulation schemes are described. The proposed protocol offers data rates scalable from 100 kbps to 870 kbps. The applicability of the protocol to both coherent and non-coherent receiver architectures is demonstrated. Link budget calculations for 30 m range are provided for both free-space and indoor propagation scenarios. The tabulated power consumption values, both at the transmitter and at the receiver, are less than 15 mW, in conformance with the technical guidance document.

Bibliography

[1] S. Lin and D. J. Costello, Error control coding., Englewood Cliffs, NJ.: Prentice-hall, 2004.

[2] P. Zhang, F. M. J. Willems and L. Huang, "Wagner-like decoding for noncoherent PPM based ultra-low-power communications," in *IEEE 24th International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC)*, London, 2013.