Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [Proposal for TBDs in TVWS-NB-OFDM draft document]
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Re: [Proposal of TVWS-NB-OFDM for IEEE 802.15.4m Document]

Abstract: [This document proposes additions and modifications of description of the TVWS-NB-OFDM section in the preliminary draft 15-12-0575-00-4m.]
Purpose: []

Summary

- This document proposes additions and modifications of description of the TVWS-NB-OFDM section in the TG4m preliminary draft 15-12-0575-00-4m.
  - 20.3.1.4 PSDU field
  - 20.3.2 System parameters for TVBS-NB-OFDM (Table 142)
  - 20.3.3.1 Reference modulator diagram
  - 20.3.3.2.2 Inner encoding
  - 20.3.3.2.3 Pad bit Insertion
  - 20.3.5.1 Operating frequency range

20.3.1.4, 20.3.2 and 20.3.5.1

- 20.3.1.4 PSDU field
  - The PSDU field carries the data of the PPDU.
- 20.3.2 System parameters for TVBS-NB-OFDM

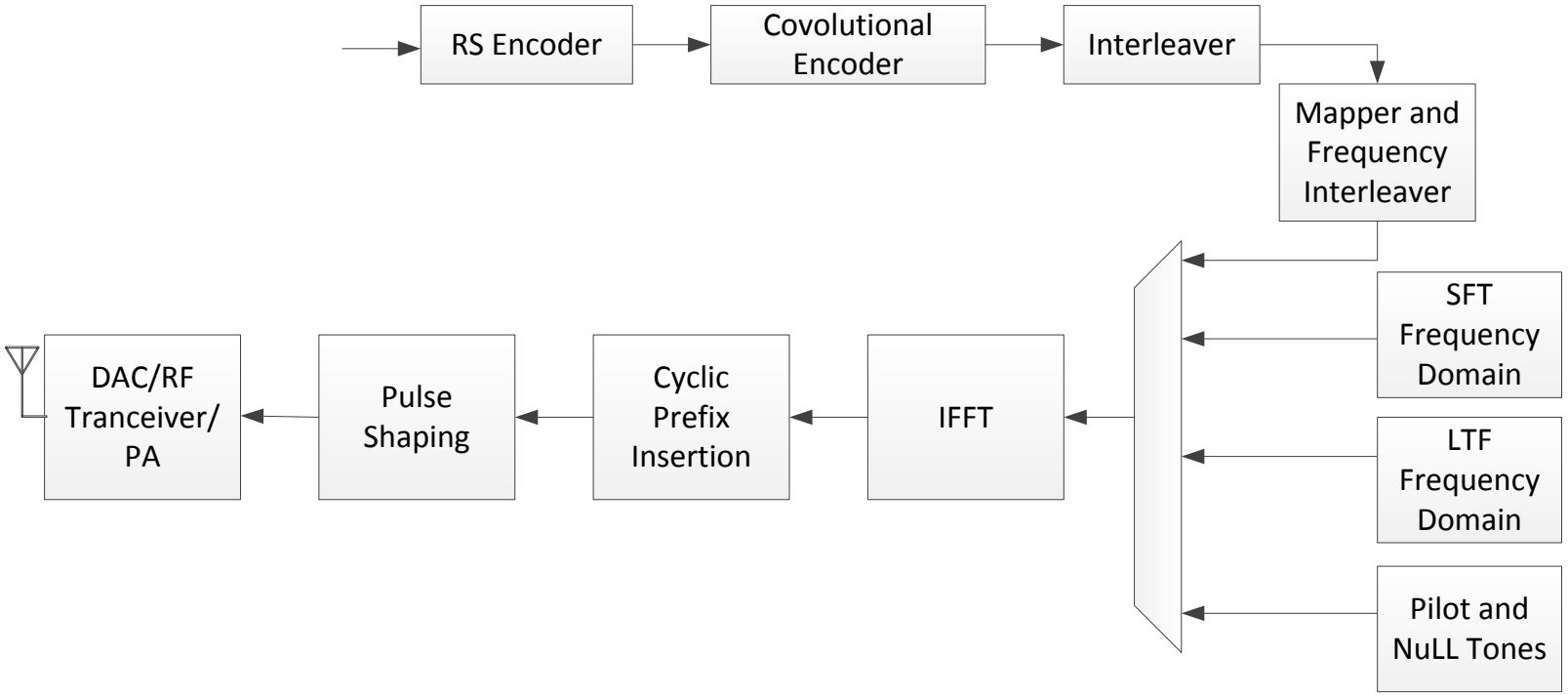
Table 142 (Continued)

Parameter	Mode #1	Mode #2
STF duration (T_{STF})	1 symbol	
LTF duration (T_{LTF})	1 symbol	

- 20.3.5.1
  - Reference Table 4 of section 5.2.4.32 in a NB-OFDM appropriate section. Use the same reference for FSK and OFDM section.

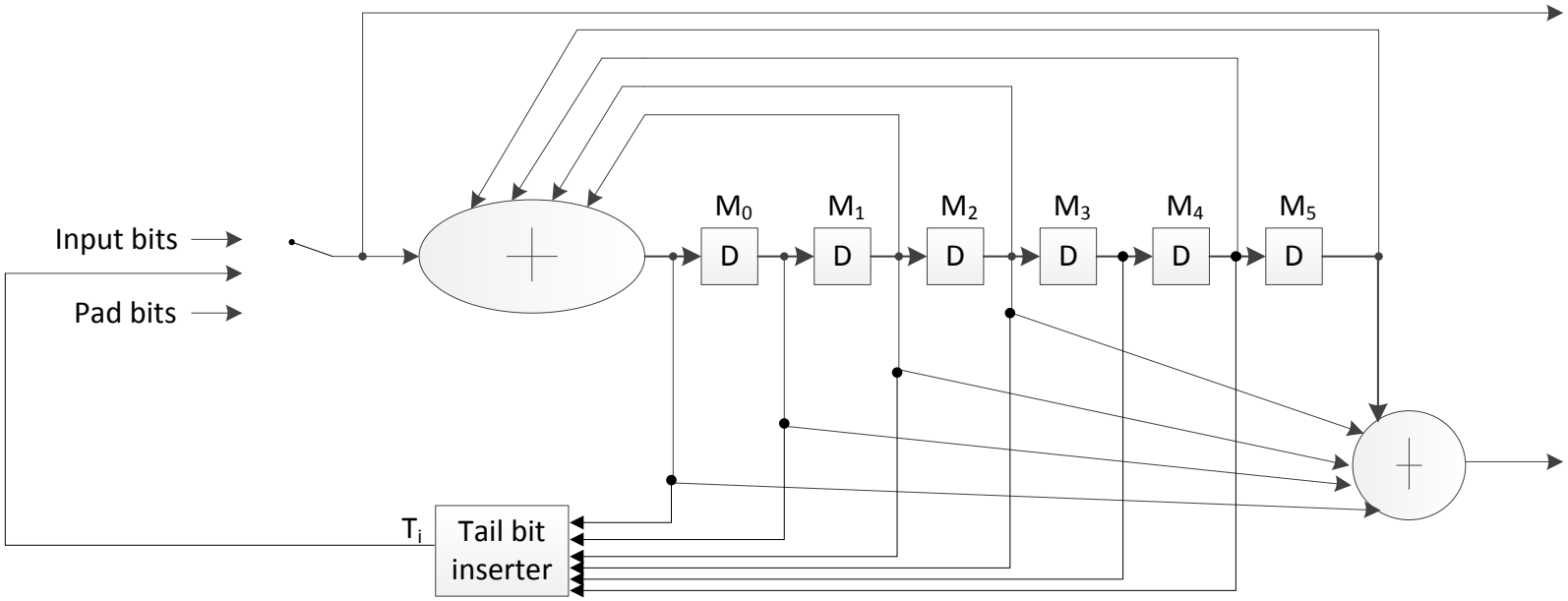
20.3.3.1 Reference modulator diagram

- The reference modulator diagram is shown in Figure zzz.



20.3.3.2.2 Inner encoding (1/2)

- A recursive and systematic convolutional encoder of coding rate R = 1/2, 2/3, 3/4, 7/8 encodes the RS encoded data bits, 6 tail bits, and pad bits. The convolutional encoder shall use the generator polynomials g0 = 171 and g1 = 133, of rate R = 1/2, with feedback connection of g0 as shown in Figure 129.



20.3.3.2.2 Inner encoding (2/2)

- The value of the tail bits are dependent on the memory state shown in Figure 129 and shall be set as shown in Table xxx.

Table xxx—Tail bit pattern for the recursive systematic encoder

Memory state (M_0–M_5)	Tail bits (T_0–T_5)	Memory state (M_0–M_5)	Tail bits (T_0–T_5)	Memory state (M_0–M_5)	Tail bits (T_0–T_5)	Memory state (M_0–M_5)	Tail bits (T_0–T_5)
000000	000000	010000	100001	100000	111011	110000	011010
000001	111001	010001	011000	100001	000010	110001	100011
000010	001011	010010	101010	100010	110000	110010	010001
000011	110010	010011	010011	100011	001001	110011	101000
000100	010110	010100	110111	100100	101101	110100	001100
000101	101111	010101	001110	100101	010100	110101	110101
000110	011101	010110	111100	100110	100110	110110	000111
000111	100100	010111	000101	100111	011111	110111	111110
001000	101100	011000	001101	101000	010111	111000	110110
001001	010101	011001	110100	101001	101110	111001	001111
001010	100111	011010	000110	101010	011100	111010	111101
001011	011110	011011	111111	101011	100101	111011	000100
001100	111010	011100	011011	101100	000001	111100	100000
001101	000011	011101	100010	101101	111000	111101	011001
001110	110001	011110	010000	101110	001010	111110	101011
001111	001000	011111	101001	101111	110011	111111	010010

20.3.3.2.3 Pad bit Insertion

The number of pad bits input to the convolutional encoder, N_{PAD}, shall be computed with to the following equation:

N_{RS} = ceiling (L_{PSDU} /(188*8))

L_{RS}= L_{PSDU}+N_{RS}×16*8

N_{SYS} = ceiling ((L_{RS} +6)/ N_{DBPS}))

N_{DATA}= N_{SYS}* N_{DBPS}

N_{PAD}= N_{DATA} - 8*L_{RS}+6

L_{PSDU} is the number of PSDU bits, which is equal to the content of the Frame Length field in Figure 128, and N_{DBPS} is shown in Table 142.

The function ceiling (.) is a function that returns the smallest integer value greater than or equal to its argument value. The pad bits are set to “zeros”.