

IEEE P802.15
Wireless Personal Area Networks

Project	IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)	
Title	Modified PHY Header	
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Re:		
Abstract	Modified PHY Header based on LB comments and contributions	
Purpose	[TG 7 received about PHY header related comments in LB. This document is the response about PHY header comments]	
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6.4 PPDU format

This clause specifies the format of the PPDU packet.

For convenience, the PPDU packet structure is presented so that the leftmost field as written in this standard shall be transmitted or received first. All multiple octet fields shall be transmitted or received least significant octet first and each octet shall be transmitted or received least significant bit (LSB) first. The same transmission order should apply to data fields transferred between the PHY and MAC sublayer.

Each PPDU packet consists of the following basic components:

- a) A SHR, which allows a receiving device to synchronize and lock onto the bit stream.
- b) A PHR, which contains frame length information.
- c) A variable length payload, which carries the MAC sublayer frame.

6.4.1 General packet format

The PPDU packet structure shall be formatted as illustrated in Figure 21.

Preamble (6.4.1.1)	Burst mode (6.4.1.3.1)	Channel number (6.4.1.3.2)	MCS ID (6.4.1.3.3)	Length of PSDU (6.4.1.3.4)	Reserved fields (6.4.1.3.5)	Dimmed OOK (6.4.1.3.6)	HCS (6.4.1.3.7)	Comp Len (Option) (6.4.1.3.8)	Resync Length (Option) (6.4.1.3.9)	Subframe Length (Option) (6.4.1.3.10)	HCS (Option) (6.4.1.3.7)	Channel estimation sequence (Option) (see 6.4.1.5)	PSDU (see 6.4.1.6)
SHR		PHR										PHY Payload	

Figure 21—Format of the PPDU

6.4.1.1 Preamble field

The preamble field is used by the transceiver to obtain chip and symbol synchronization with an incoming message. The standard defines one fast locking pattern followed by choice of 4 preambles for the purposes of distinguishing different PHY topologies.

The preamble first starts with a fast locking pattern of at least 64 alternate 1's and 0's. This maximum transition sequence provides the ability to lock the clock and data recovery circuit in the quickest time. The fast locking pattern length shall not exceed 16384 bits. Before the clock and data recovery (CDR) attains lock and recovers the clock, it has no way of determining the logic value of the transmitted sequence. After the fast locking pattern, 4 repetitions of one of four preambles are sent.

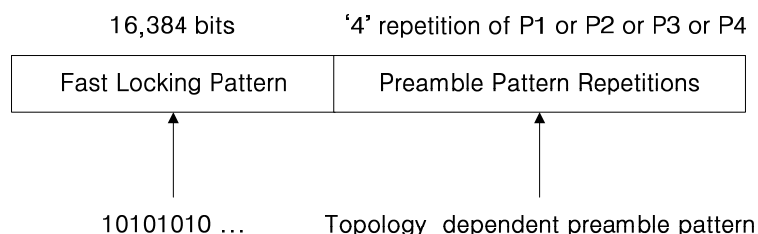


Figure 23 – Default preamble transmission

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P1 : 1 1 1 1 0 1 0 1 1 0 0 1 0 0 0
P2 : 0 0 1 0 1 1 1 0 1 1 1 1 1 1 0
P3 : 1 0 0 1 1 0 0 0 0 0 1 0 0 1 1
P4 : 0 1 0 0 0 0 1 1 0 1 0 0 1 0 1

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Figure 24 – Preambles for various topology modes

The preamble of Figure 24 shall be transmitted using an OOK modulation. If there are multiple light sources supported by the device, all light sources shall transmit the same preamble simultaneously.

It is also acceptable to invert the proposed preamble sequences and transmit; that is, the PHY can select whether to transmit each preamble sequence or its inversion. The advantage of doing this is that this allows for two preamble sequences to be searched for simultaneously at the receiver for a given MAC operating mode and allow co-existence of two piconets in a given operating mode, without any increase in complexity.

The same preamble sequences are used for low rate and high rate PHY. The number of repetitions of the fast locking pattern can be extended by the MAC during idle time or for different operating modes for better synchronization or to provide visibility or image array device discovery.

P1 can be used with any topology and can also be used for visibility support frames.

6.4.1.2 Preamble for burst mode

The fast locking pattern can be dropped for the burst mode since it is already synchronized to the transmitter. This reduces the preamble length by half and provides higher throughput at the MAC layer.

Table 21—Preamble for MAC operation code

Preamble	Topology operating mode
P1 or inverted P1	topology independent
P2 or inverted P2	peer to peer
P3 or inverted P3	star
P4 or inverted P4	broadcast

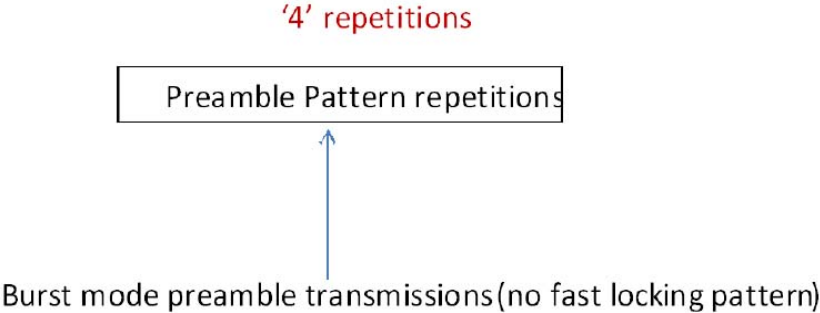


Figure 25—Burst preamble transmission

6.4.1.3 PHY header

The header, as shown in Table 23, shall be transmitted with an OOK modulation. If there are multiple light sources supported by the device, all light sources shall transmit the same header contents simultaneously. The band plan ID field in this case shall be that of the lowest band plan ID.

Table 23—PHY Header

PHY header fields	Bit width	Explanation on use
Burst mode	1	Reduce preamble and IFS
Channel number	3	Band plan ID
MCS ID	6	Provide information on PHY type and data rate
Length of PSDU	16	Length up to aMaxPHYPacketSize (Table 24)
Dimmed OOK	1	Info on comp time, resynch and length of sub-frame
Reserved fields	5	Future use
HCS	16	Header check sequence

Table 23a— Dimmed OOK Extension (applicable only if Dimmed OOK =1)

PHY header fields	Bit width	Explanation on use
Compensation Length	10	Compensation length in Optical Clocks
Resynch Length	4	Number of resync optical clocks
Subframe Length	10	Length of sub-frame in optical clocks
HCS	16	Header check sequence

6.4.1.3.1 Burst mode

The burst mode bit is for the next packet. It indicates that next packet is burst mode. Refer to 6.4.1.2 Preamble for burst mode for more detailed information.

6.4.1.3.2 Channel number

Channel number is code in Table 1. The codes in Table 1 are used to indicate the frequency band containing the spectral peak (energy) for the transmitted packet. Refer to 6.1.2 Operating frequency range and channel assignments for more detailed information

6.4.1.3.3 MCS ID

Table 24— MCS ID table

	MCS Indication	PHY	Data rate	Unit
0	000000	I	11.67	kbps
1	000001	I	24.44	kbps
2	000010	I	48.89	kbps
3	000011	I	73.3	kbps
4	000100	I	100	kbps
5	000101	I	35.56	kbps
6	000110	I	71.11	kbps
7	000111	I	124.4	kbps
8	001000	I	266.6	kbps
16	010000	II	1.25	Mbps
17	010001	II	2	Mbps
18	010010	II	2.5	Mbps
19	010011	II	4	Mbps

20	010100	II	5	Mbps
21	010101	II	6	Mbps
22	010110	II	9.6	Mbps
23	010111	II	12	Mbps
24	011000	II	19.2	Mbps
25	011001	II	24	Mbps
26	011010	II	38.4	Mbps
27	011011	II	48	Mbps
28	011100	II	76.8	Mbps
29	011101	II	96	Mbps
32	100000	III	12	Mbps
33	100001	III	18	Mbps
34	100010	III	24	Mbps
35	100011	III	36	Mbps
36	100100	III	48	Mbps
37	100101	III	72	Mbps
38	100110	III	96	Mbps
others	others	Reserved	Reserved	

6.4.1.3.4 Length of PSDU

The PSDU length field is 16 bits in length and specifies the total number of octets contained in the PSDU (i.e. PSDU). It is a value between 0 and *aMaxPHYPacketSize* as shown in 6.5.1

6.4.1.3.5 Reserved fields

6.4.1.3.6 Dimmed OOK

The dimmed OOK bit shall be set to one when supporting dimming while using OOK modulation. This bit indicates that 3 more fields are present at the end of the header. These fields are described in 6.4.1.3.8, 6.4.1.3.9 and 6.4.1.3.8. The three added fields have their own HCS post-appended.

6.4.1.3.7 HCS

The PHY header shall be protected with a 2 octet CRC-16 header check sequence (HCS). A schematic of the CRC processing is shown in annex J. The HCS bits shall be processed in the transmit order. The registers shall be initialized to all ones.

6.4.1.3.8 Compensation Length

The compensation length has a 10 bit value which indicates the number of compensation symbols at the optical clock rate. The values of these symbols are user defined. When used this field shall be set to a value from 0 to 1023.

6.4.1.3.9 Resynch Length

The resynch length has a 4 bit value which indicates the number of resynch symbols at the optical clock rate. The resynch pattern is the same as the preamble. When used this field shall be set to a value from 0 to 15.

6.4.1.3.10 Subframe Length

The subframe length has a 10 bit value which indicates the number of uncoded data bits in the subframe. When used this field shall be set to a value of 0 to 1023.

6.4.1.3.10.1 Subframe Generation

When used, the subframes shall be generated at the transmitter after the FCS has been determined and the FEC has been applied. That is, the FEC and FCS shall not include the compensation symbols and the resync symbols.

6.4.1.4 Channel estimation sequence

The channel estimation sequence is optional and is used in PHY Type 3. The information about PHY type 3 is obtained after decoding the PHY header. The length of channel estimation sequence is 8 bit. Refer to 6.8.6.1 CSK Calibration for more detailed information.

6.4.1.5 PSDU field

The PSDU field has a variable length and carries the data of the PHY packet.