Improved PHR coding of the MR-O-QPSK PHY

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Re:	Task Group 15.4g LB51 comment resolution
Abstract:	Comment resolutions related to PHR coding of the MR-O-QPSK PHY
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Motivation

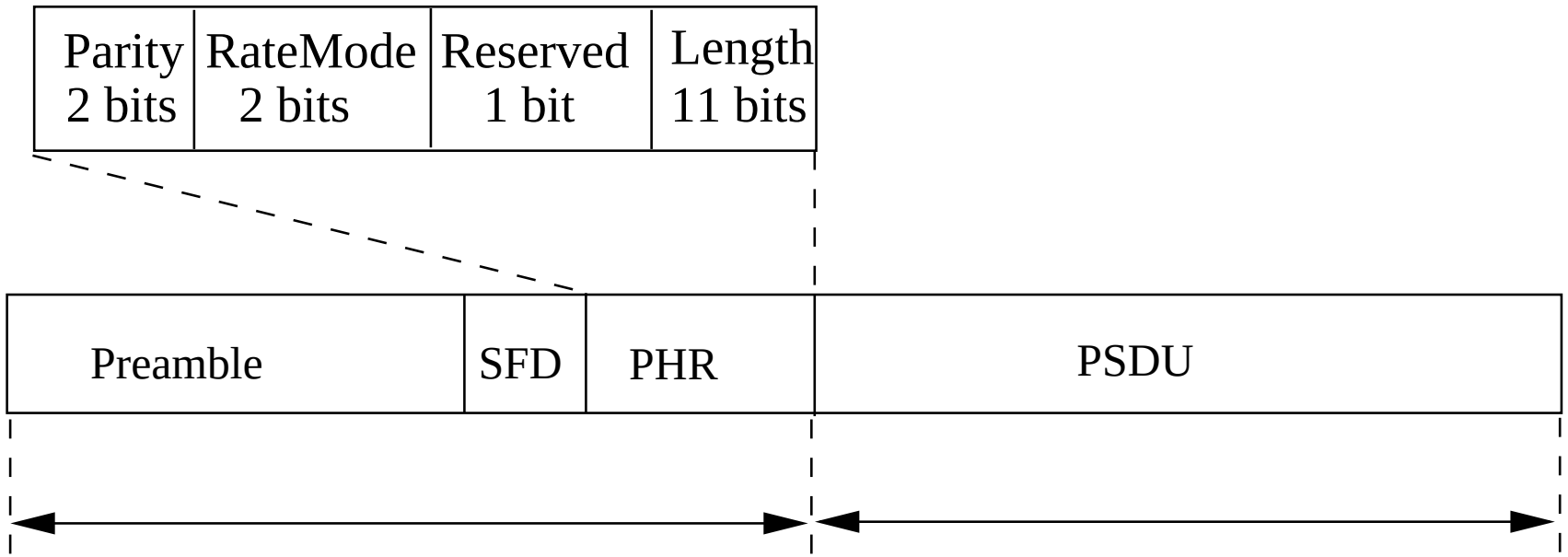
This document describes the proposed resolution of LB51 on some comments related to MR-O-QPSK PHY regarding the PHY header (PHR).
The following comments are addressed:

- SFD length: CID # 879
- PHR error detection: CID # 890, 891, 912
- PHR FEC: CID # 1470

The following comments are partially addressed:

- Pilot sequences: CID # 1475

Coding of PPDU scheme (780/915 MHz band)[1]



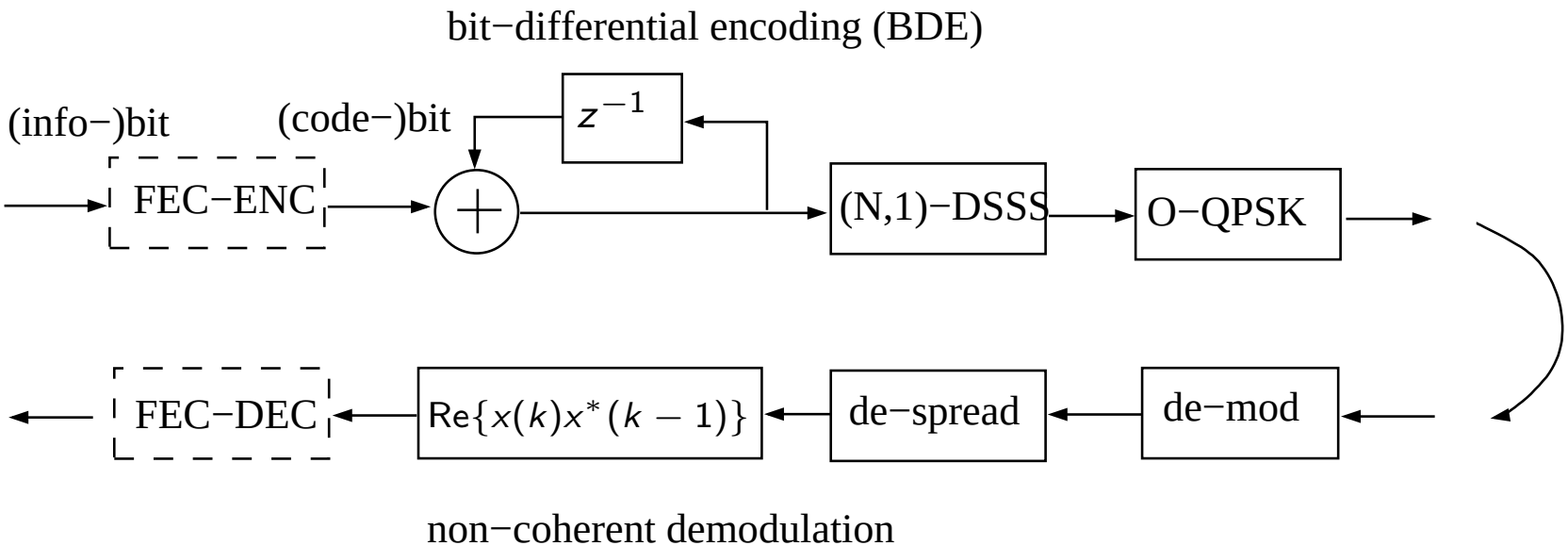
[1] as specified for the MR-O-QPSK PHY in draft P802.15.4g/d1,March 2010

- Bits of Preamble, SFD and PHR field:
  - no FEC
  - bit-differential encoding (BDE)
  - (N*4,1)-DSSS
- Bits of the PSDU for the lowest data rate are:
  - FEC: rate 1/2 convolutional coding, $K = 7$
  - bit-differential encoding (BDE)
  - (N,1)-DSSS

(SHR,PHR) and PSDU are approx. balanced with regard to the BER.

So why is there an issue?

Purpose of bit-differential encoding (BDE)



Purpose of bit-differential encoding (BDE)

- low chip SNR
- exploit non-coherent detection
- no phase control loop required
- Note: at low SNR, a phase control loop may cause considerable noise enhancement.
- non-coherent demodulation after de-spreading in order to improve multi-path robustness

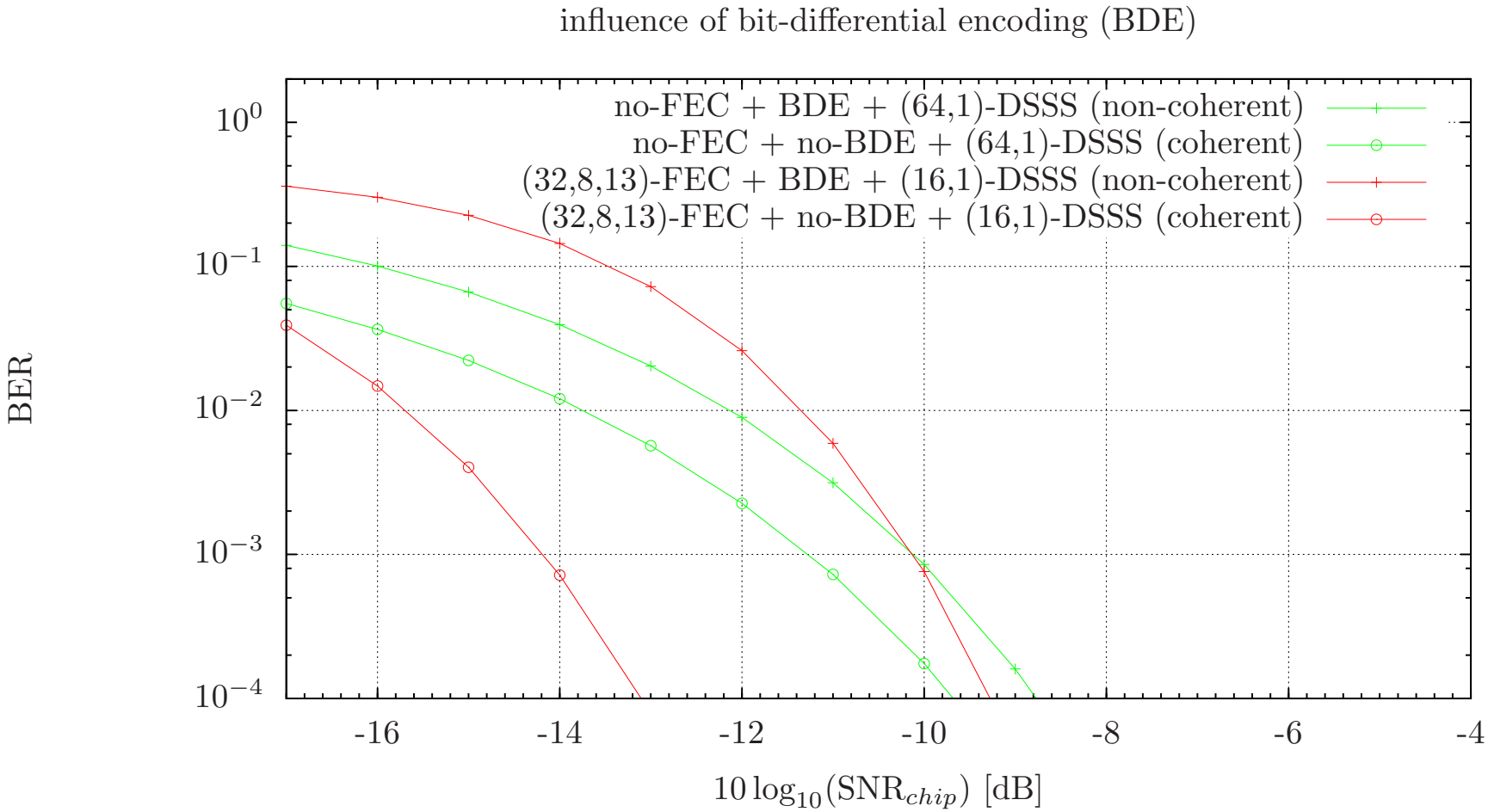
Consider a binary (32,8,$d_{min} = 13$) block code[2]

- code rate is 1/4
- optimal[3] minimum distance for a binary (32,8) linear code
- Soft-decision ML-decoding at moderate complexity (256 codewords only)

[2]This code can be obtained from a (33,8,14)-code by puncturing position 33; see T. Helleseth & Ø. Ytrehus, How to find a [33,8,14] code, Report in Informatics (preliminary version), Dept. of Informatics, Univ. of Bergen, Norway, Nov. 1989.

[3]see Markus Grassel `http://www.codetables.de/`

Simulation, assuming perfect chip synchronization and phase[4]



[4] relevant for coherent detection

- There seems to be little performance difference between:

  no-FEC + BDE + (4*N,1)-DSSS

  and

  (32,8,13)-FEC + BDE + (N,1)-DSSS
- All coding gain is eaten up by enhanced noise due to reduced spreading length.

But there is a gain!

- For real world applications, there is always a frequency offset

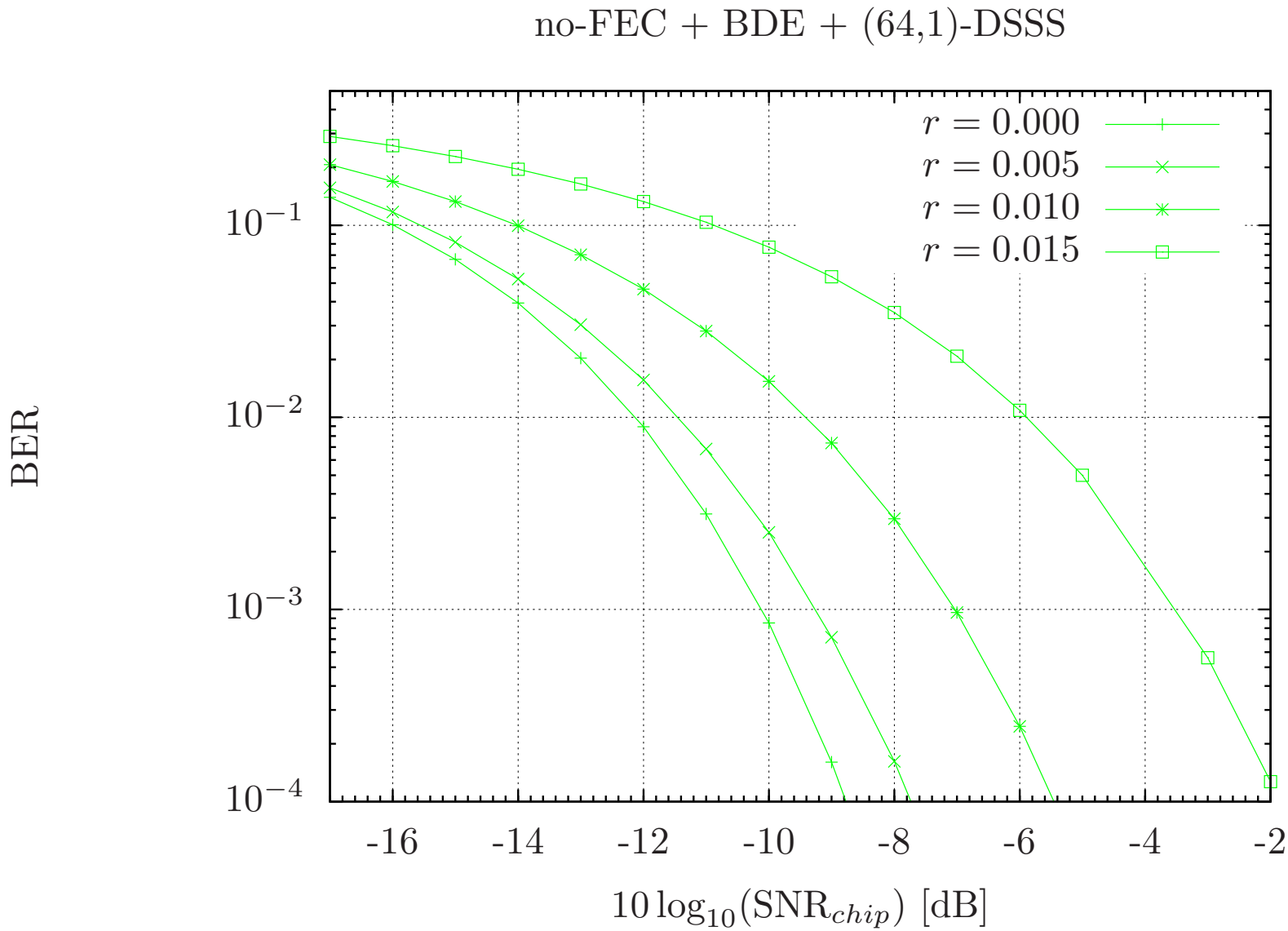
$$\Omega \ [\ \text{rad}/T_{chip}]$$

  which cannot be perfectly estimated.
- A residual frequency offset $r = \Omega - \hat{\Omega}$ causes phase drift

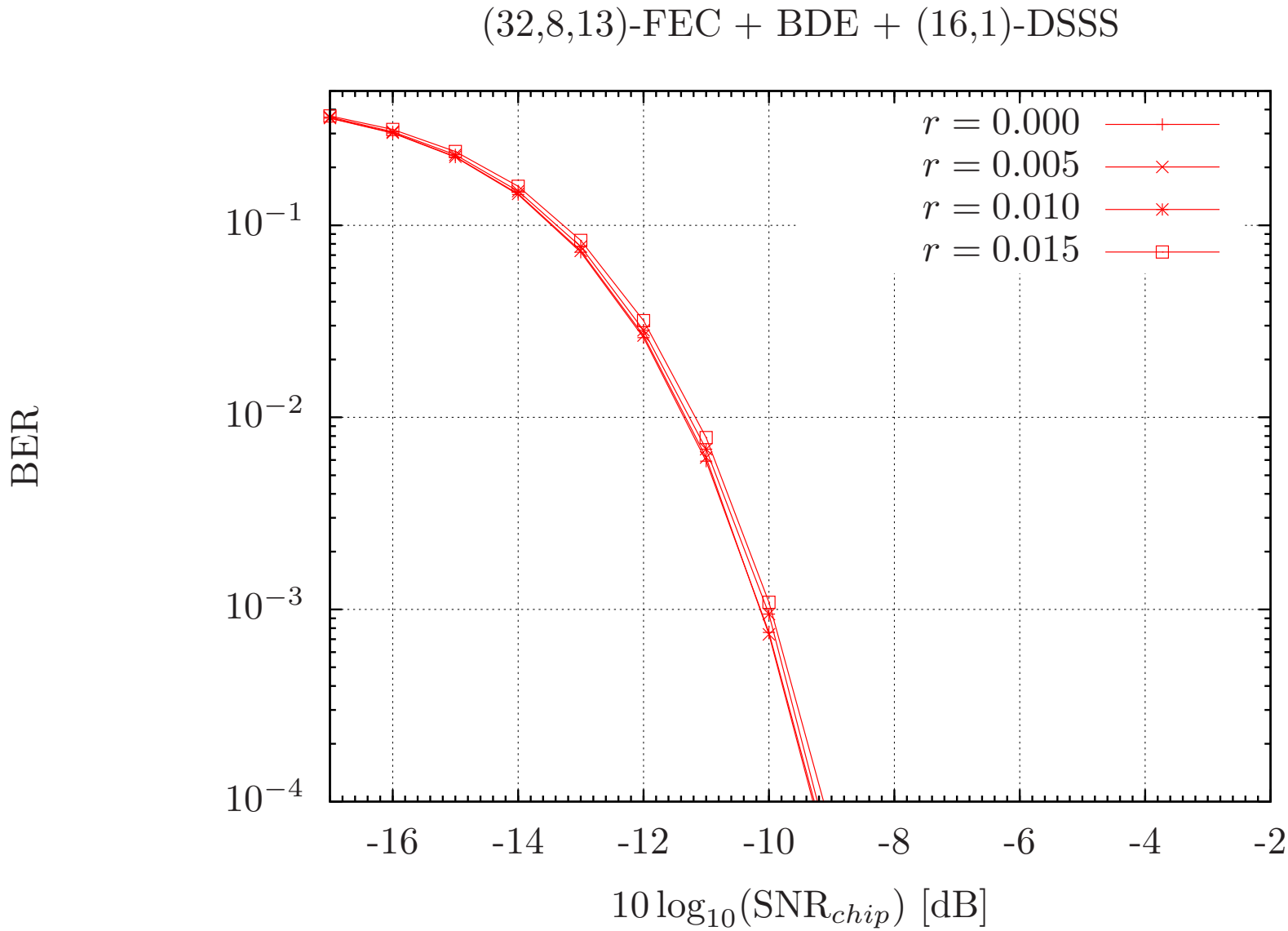
$$\tilde{x}(k) = exp(jrk)x(k)$$

- Depending on r, de-spreading will result in loss of processing gain, when de-correlating against the known chip sequence.
- Clearly, a long DSSS sequence is prone to a residual error r.

Influence of residual frequency offset $r = \Omega - \hat{\Omega}$



Influence of residual frequency offset $r = \Omega - \hat{\Omega}$



What about the SFD?

- FEC cannot be conveniently applied to the SFD.
- Will this make PHR FEC useless?

Difference between SFD and PHR field

- During PHR detection, a single info-bit error (or more) usually causes a packet error.
- During SFD detection, a single info-bit error (or more) must not lead to a packet error.

Let A_D be the event a correctly received word of length M

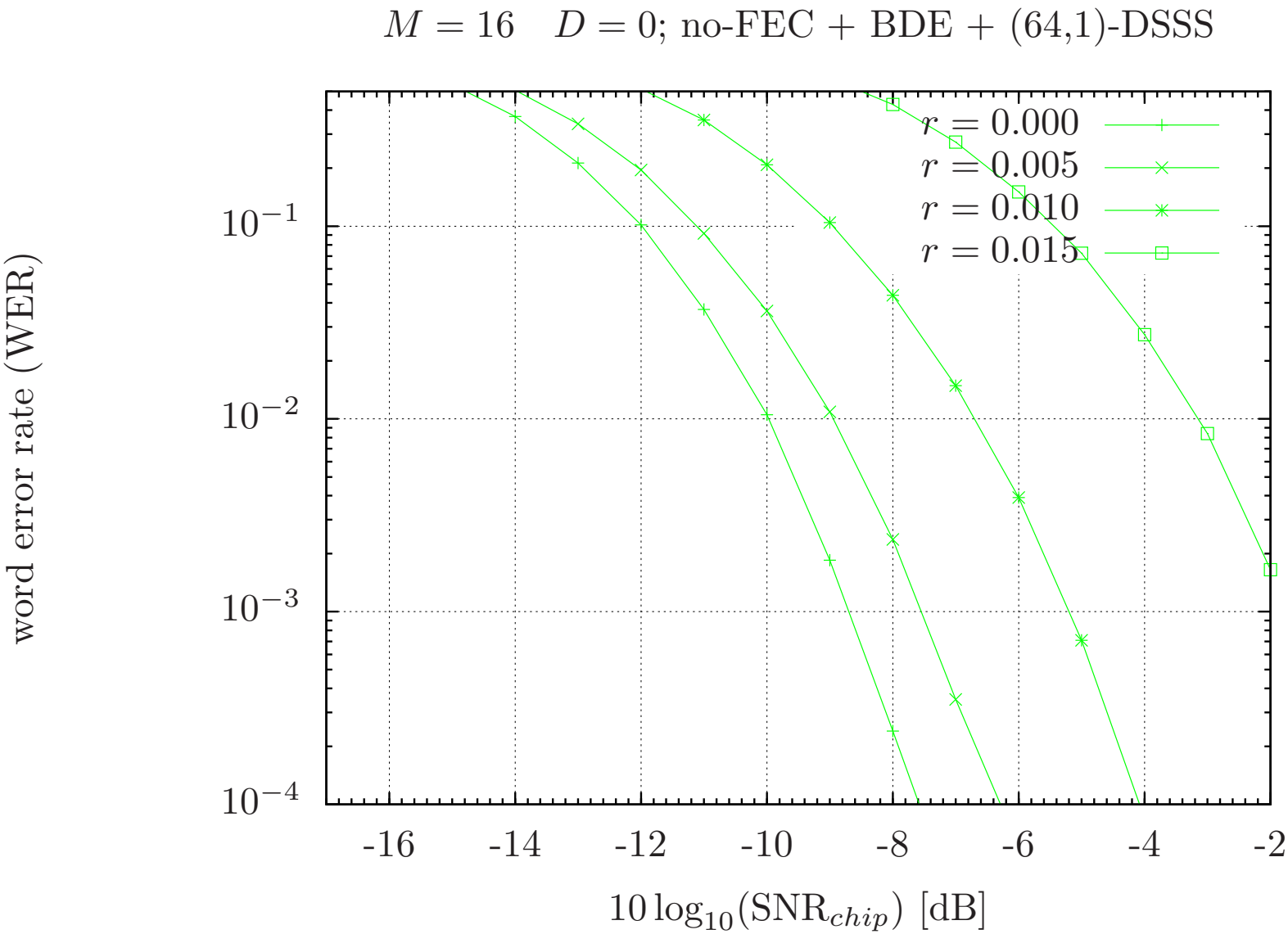
$$A_D : \|w - \hat{w}\| \leq D$$

where

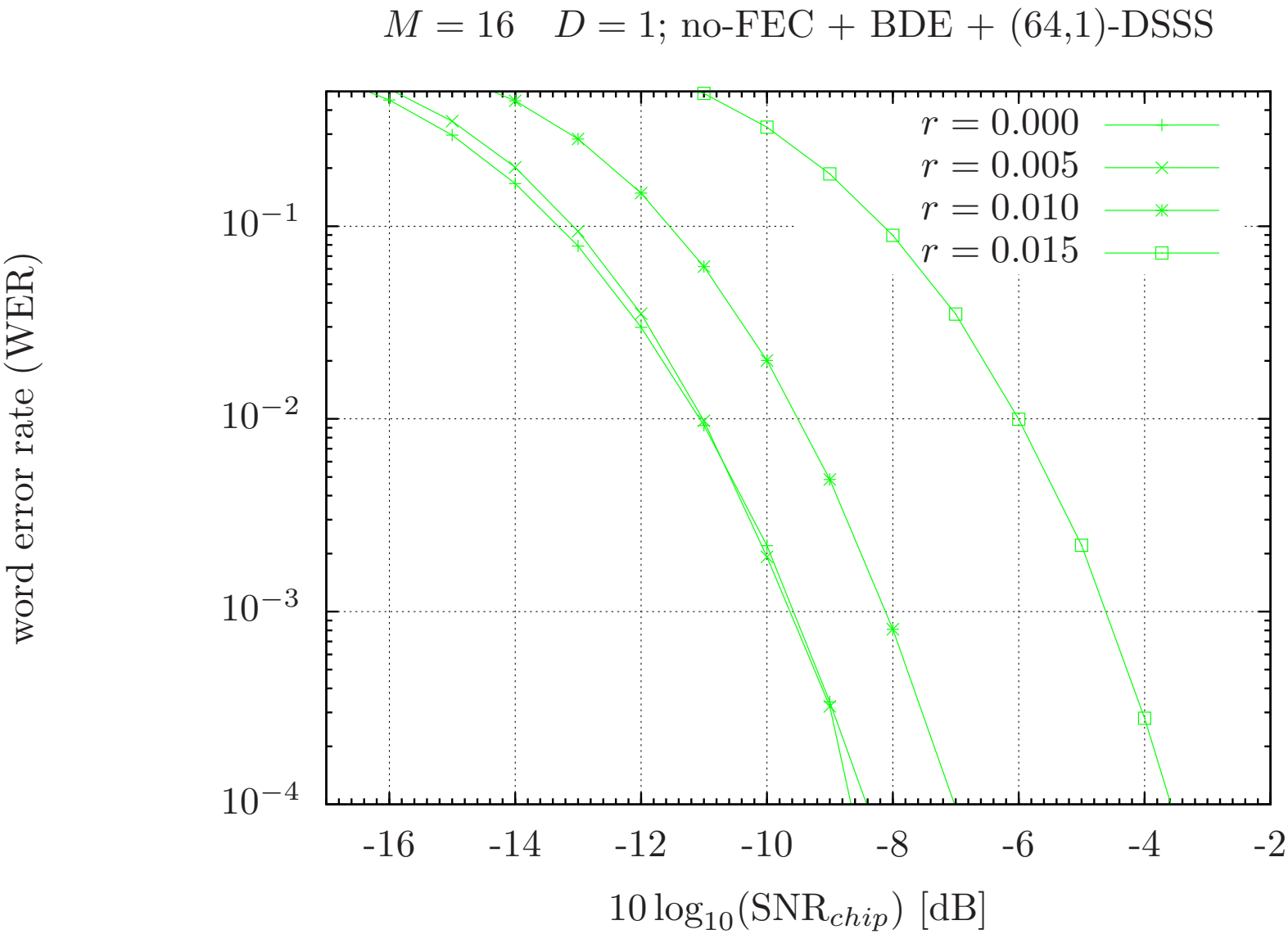
- $\|.\|$ is the Hamming distance
- $w \in GF(2^M)$ is transmitted word
- $\hat{w} \in GF(2^M)$ is the detected word
- D is the maximum number of allowed bit errors

The complementary event $\overline{A}_D$ is called a word error.

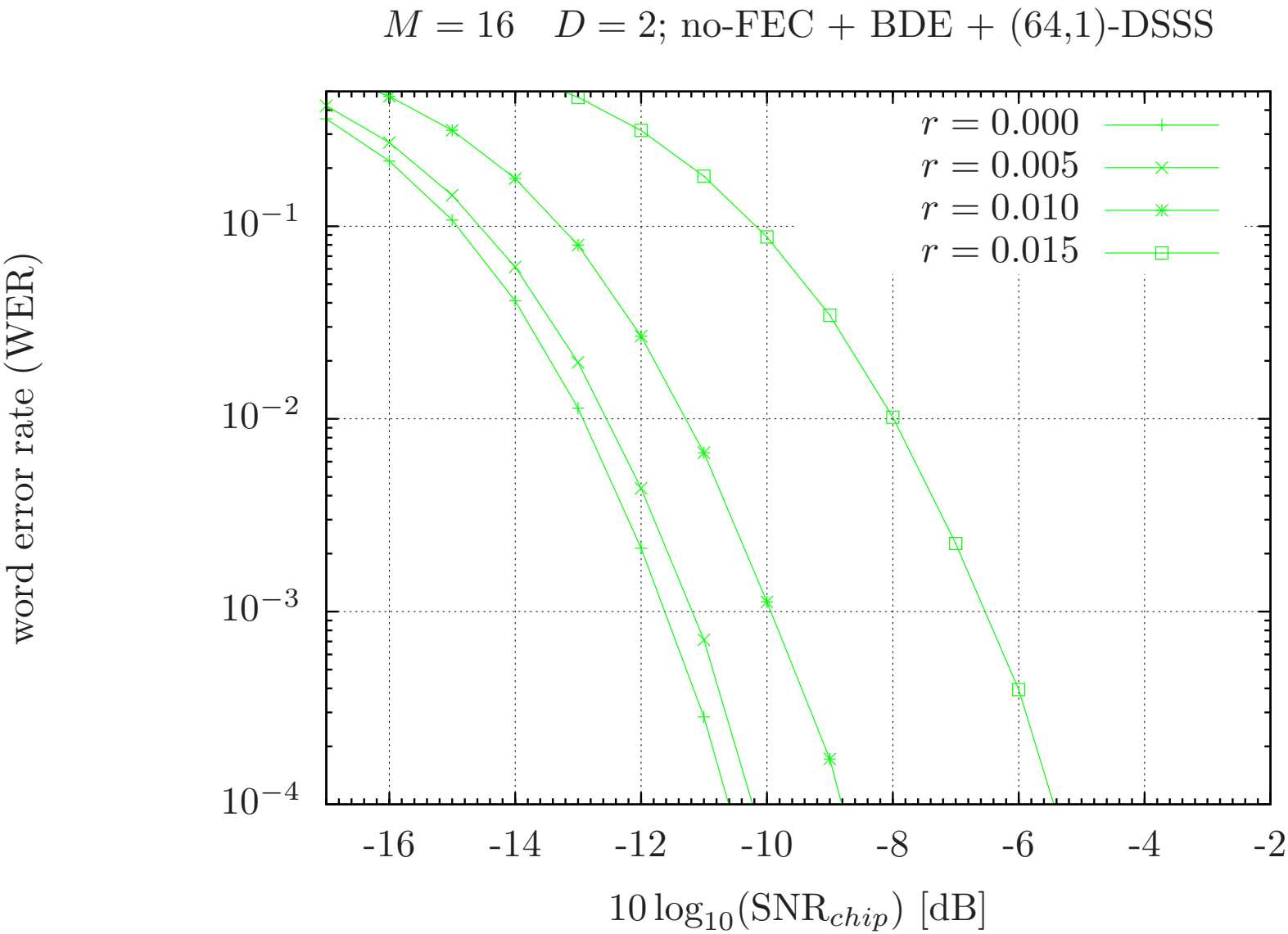
Word Error Rate (WER) for $D = 0$



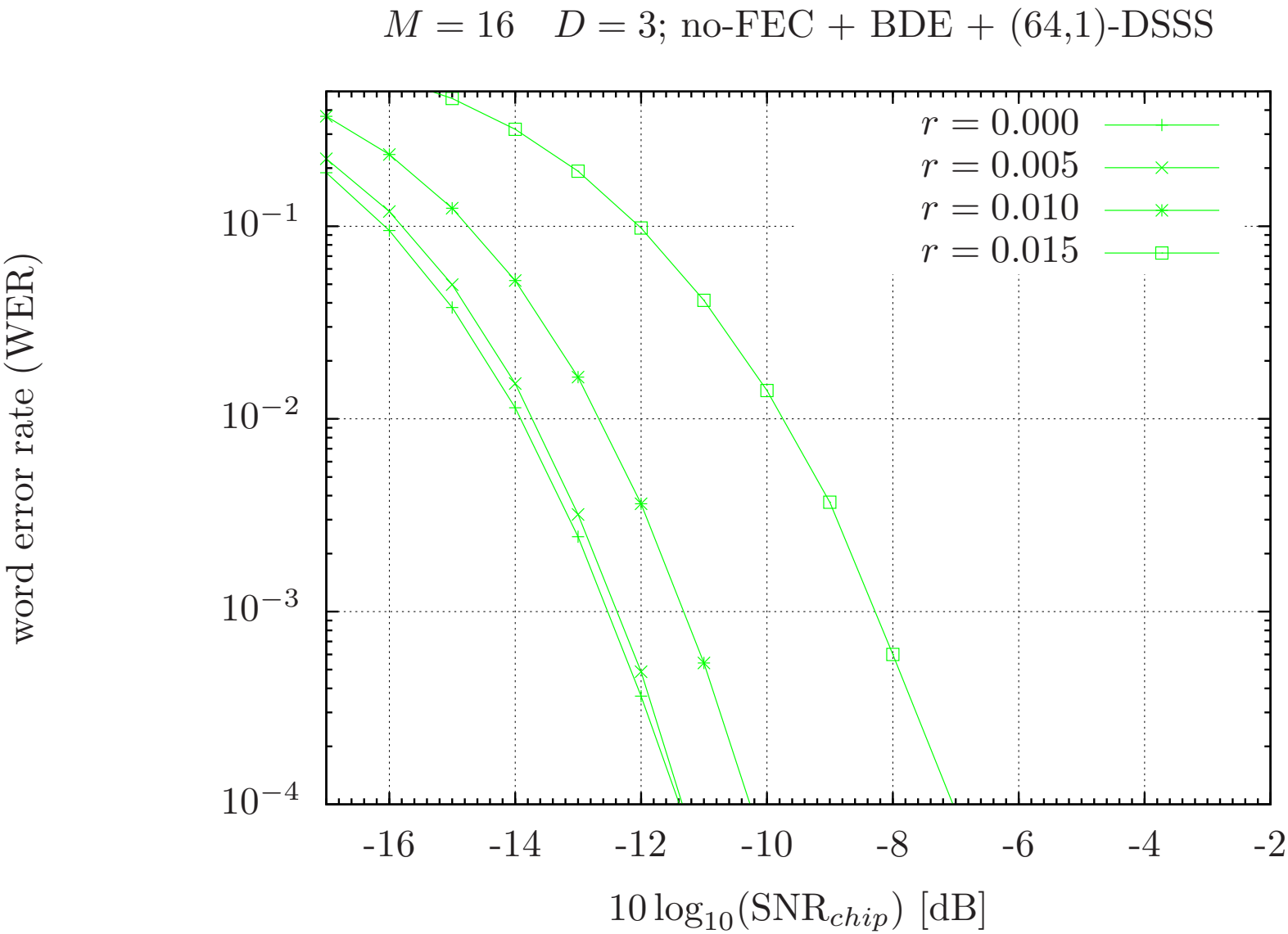
Word Error Rate (WER) for $D = 1$



Word Error Rate (WER) for $D = 2$



Word Error Rate (WER) for $D = 3$



SFD candidates

- $M = 16$ bit rather than $M = 8$ bit SFD
- In order to allow bit errors during SFD search while preserving a low false alarm rate, the Hamming distance to zero-bit preamble sequence needs be optimized:

$$w^{opt} = \underset{w \in GF(2^M)}{\text{arg-max}} \left\{ \min_{k \in 1,\ldots,M} \| w - (\underbrace{0, \ldots, 0}_{k}, w_0, \ldots, w_{M-k-1}) \| \right\}$$

For an SFD pair, two such SFD words need to be found with good Hamming distances to each other.

SFD candidates

- single[5] SFD

$$(w_0, w_1, ..., w_{15})^{opt} = (1, 1, 1, 0, 1, 0, 1, 1, 0, 1, 1, 0, 0, 0, 1, 0)$$

During search, distance to preamble is ≥ 9.

- good SFD pair

$$\begin{aligned}(w_0, w_1, ..., w_{15})^{opt} &= (1, 1, 1, 0, 1, 0, 1, 1, 0, 1, 1, 0, 0, 0, 1, 0)\\ (w_0, w_1, ..., w_{15})^{opt2} &= (1, 1, 1, 1, 0, 1, 0, 1, 1, 0, 0, 1, 0, 0, 0, 0)\end{aligned}$$

During search, distance to preamble is ≥ 8 and $\|w^{opt} - w^{opt2}\| = 9$.

[5] SpreadingMode $\in$ {DSSS,MDSSS} cannot be indicated by the SFD value.

Candidates for PHR coding and spreading (780/915 MHz band)

Scheme	# bits	FEC	Intrl.	CRC-8	DSSS	# chips
no-FEC-16-bit[6]	16	no	no	no	(64,1)	1024
no-FEC-24-bit	24	no	no	yes	(64,1)	1536
BC-16-bit	16	(32,8,$d_{min} = 13$)[7]	no	no	(16,1)	1024
BC-24-bit	24	(32,8,$d_{min} = 13$)	no	yes	(16,1)	1536
CC-32-bit	32	1/2 CC[8] $K = 7$	yes(8x8)	yes	(16,1)	1024
CC-24-bit	24	1/2 CC $K = 7$	yes(10x6)	yes	(16,1)	960
BCH-16-bit	16	BCH[9] (63,16,$t = 11$)	no	no	(16,1)	1008

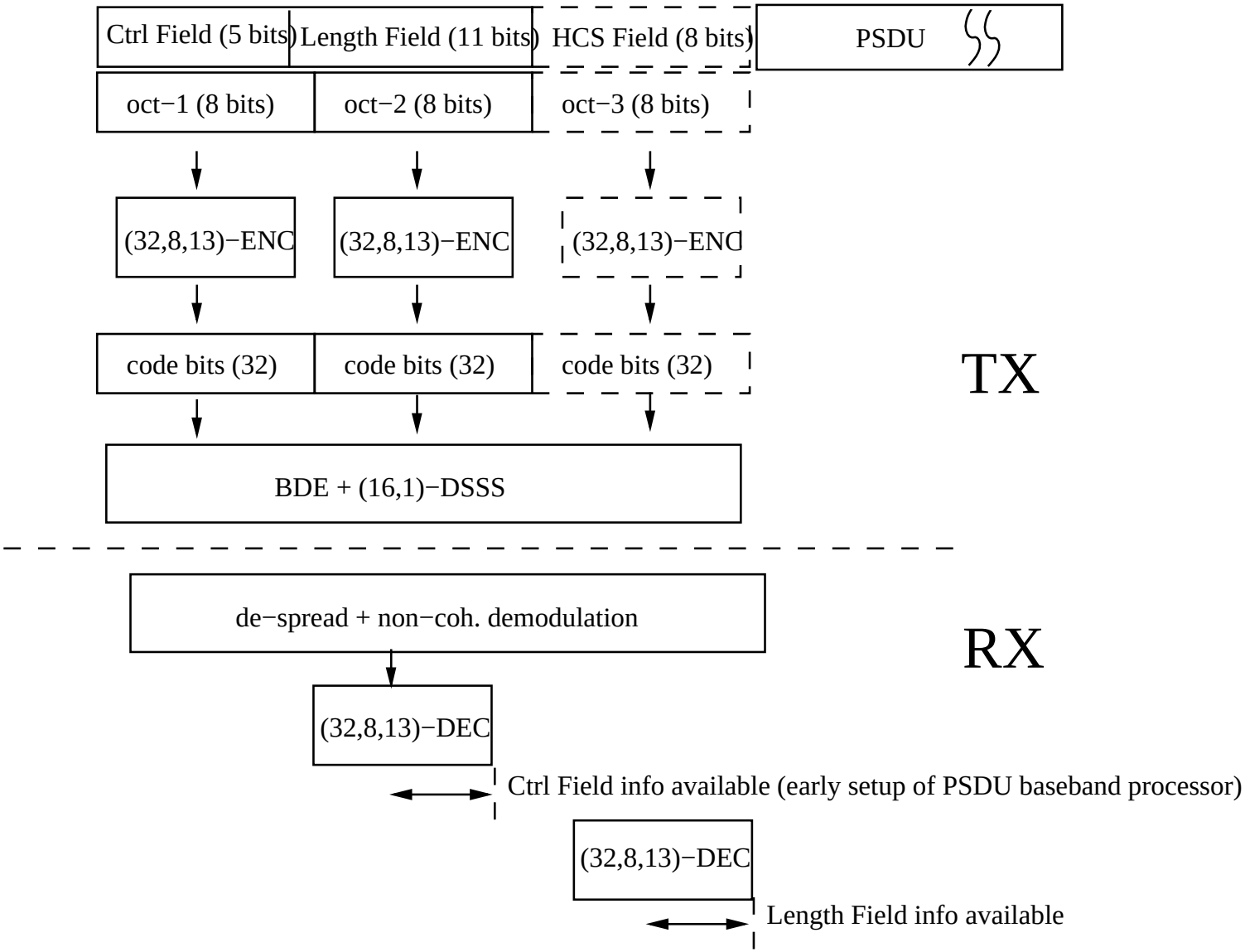
[6] as specified in draft P802.15.4g/d1,March 2010

[7] applying ML-decoding with soft decisions on code bits

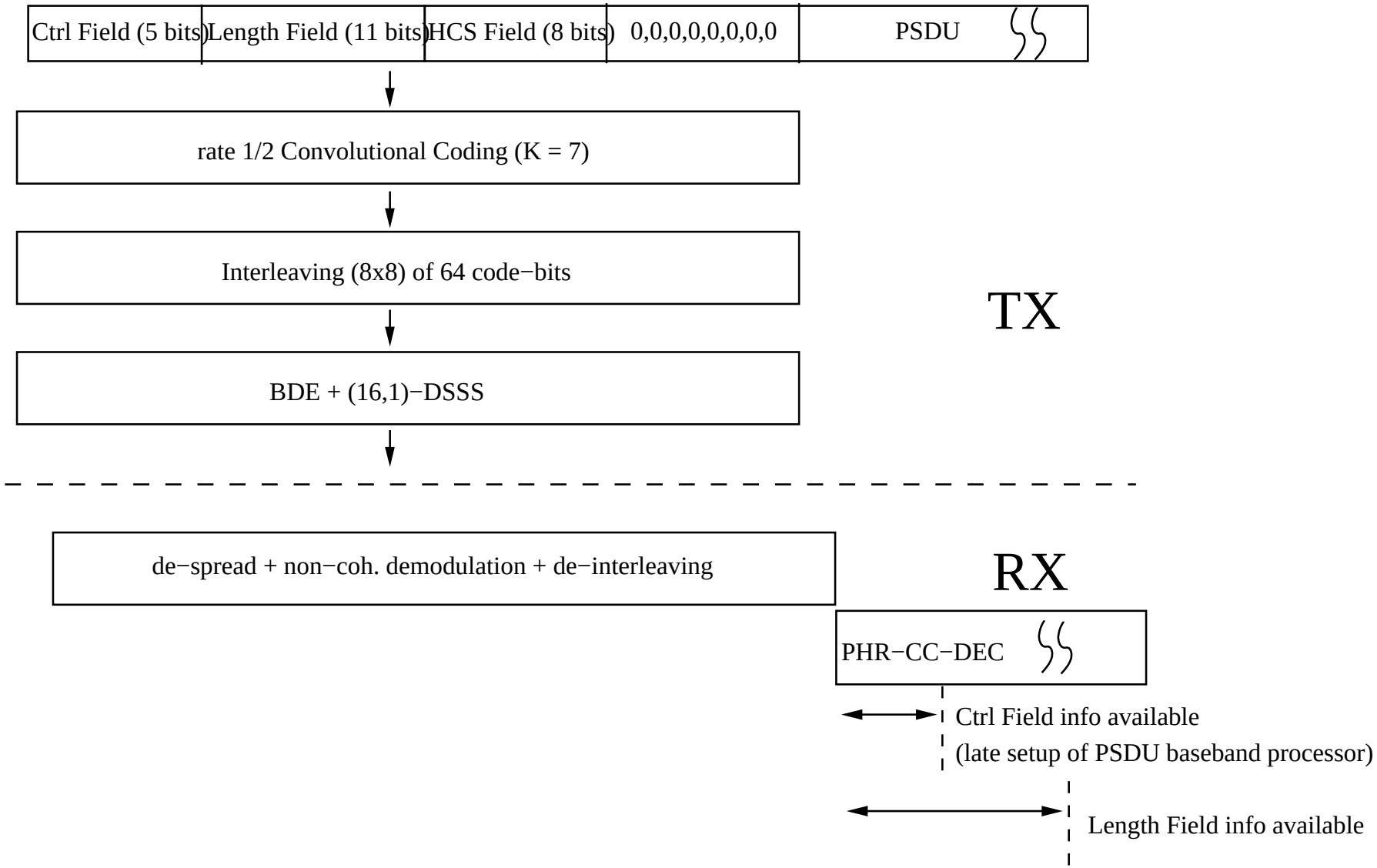
[8] applying ML-Viterbi decoding with soft decisions on code bits

[9] applying usual bounded minimum distance decoding with hard decisions on code bits

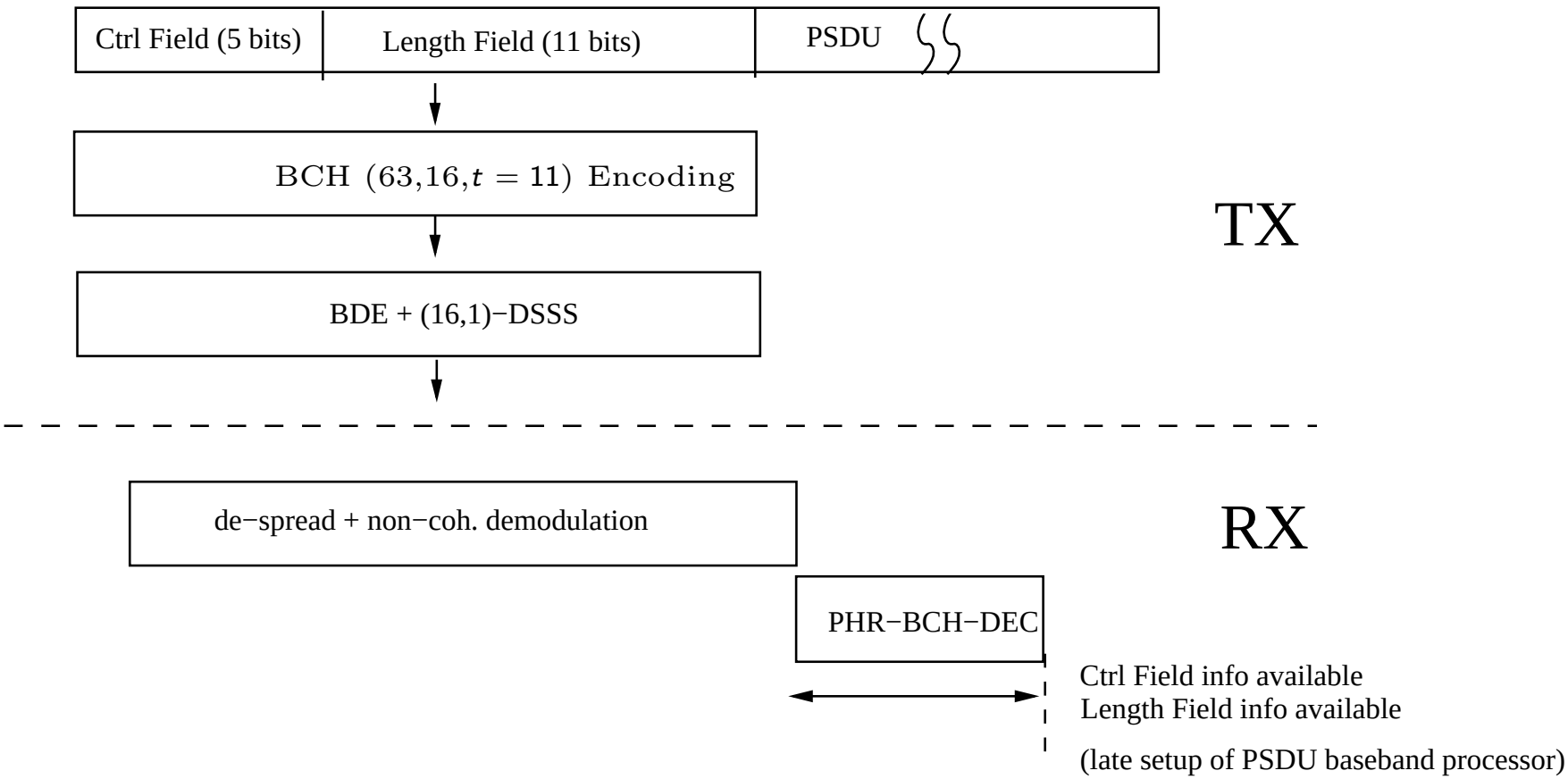
BC-16/-24-bit: Rate 1/4 (32,8,13) Block Coding



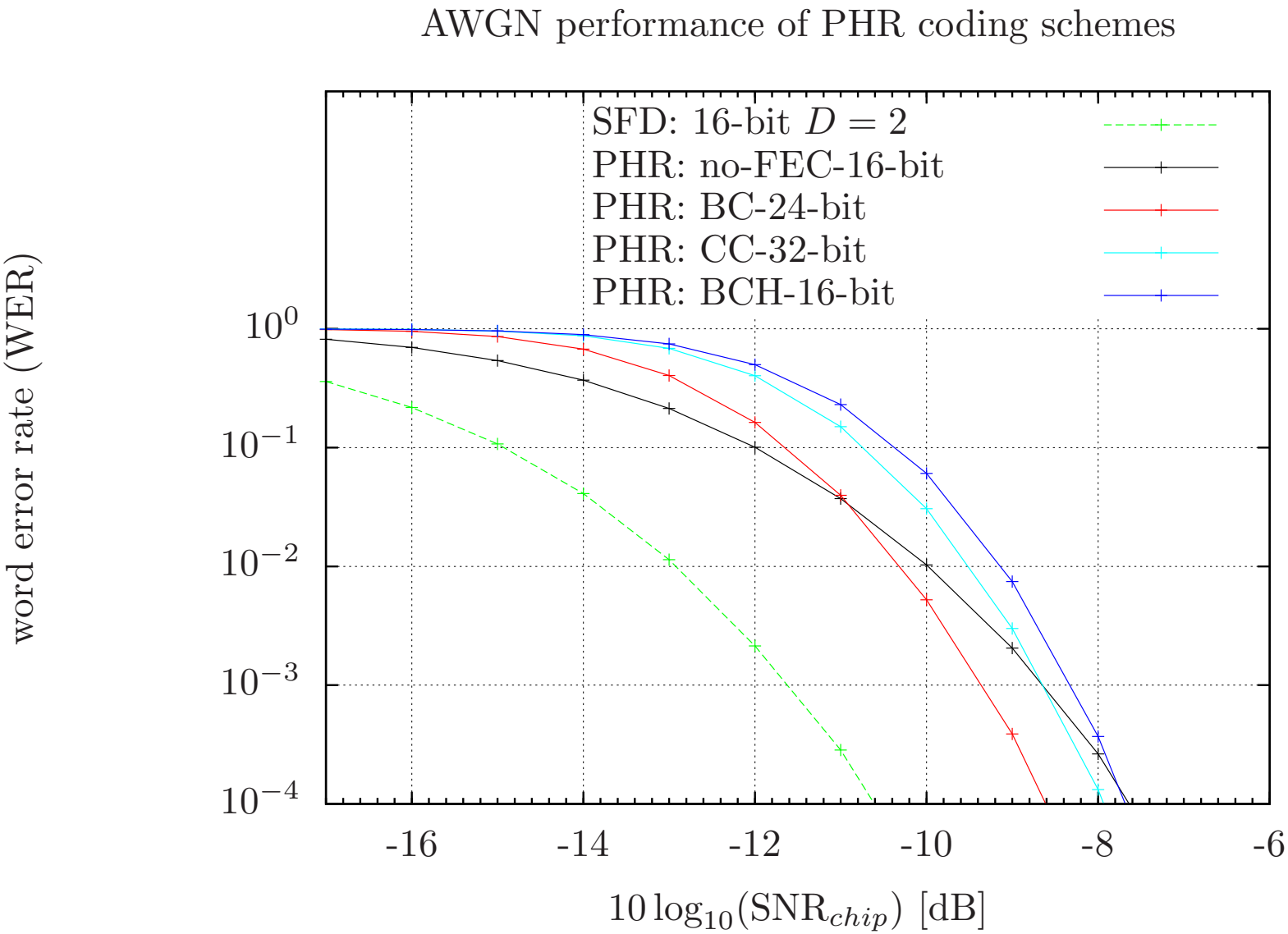
CC-32-bit: Rate 1/2 Convolutional Coding with $K = 7$



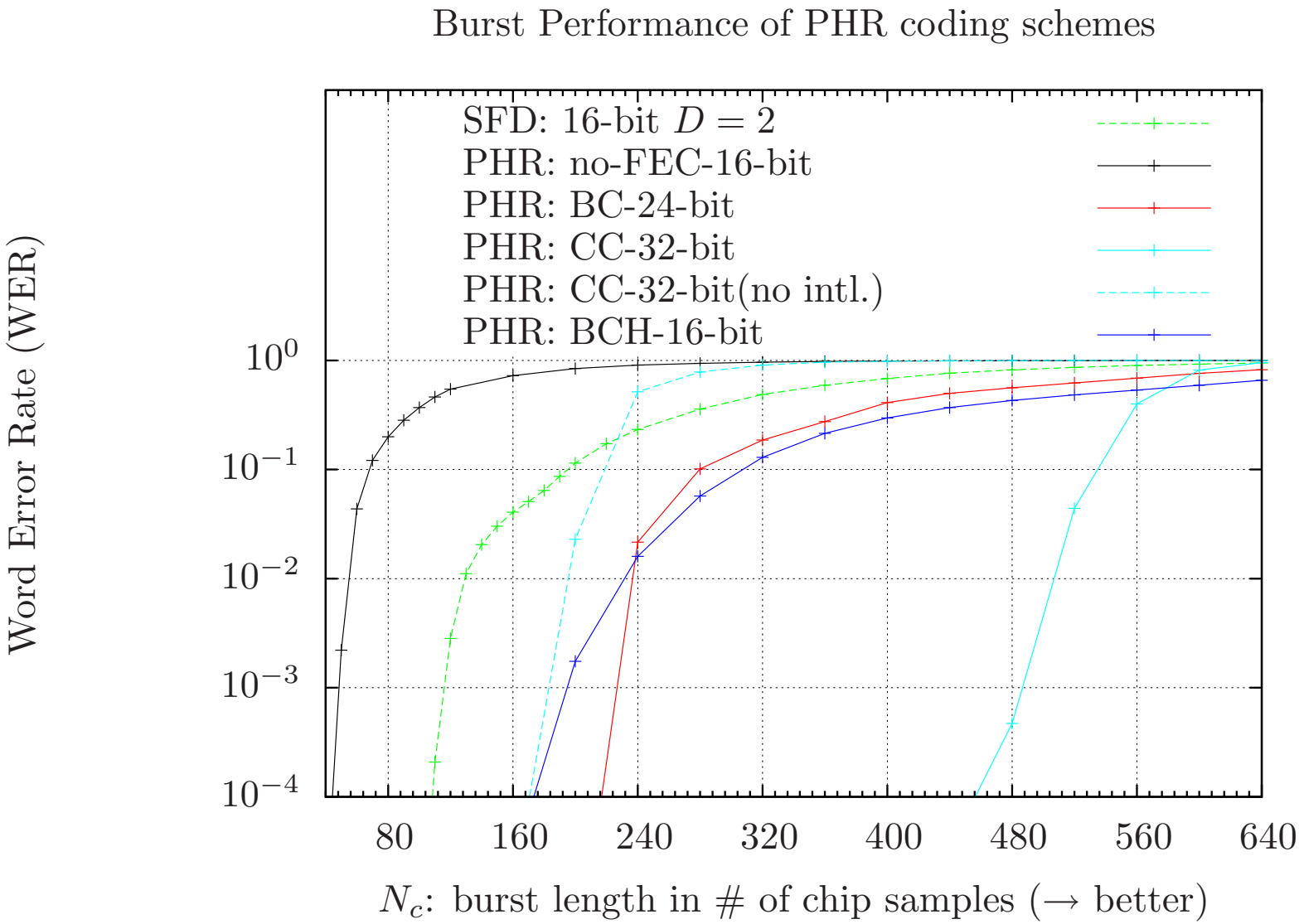
BCH-16-bit: BCH (63,16,$t = 11$)



AWGN


AWGN performance of PHR coding schemes
SFD: 16-bit $D = 2$
PHR: no-FEC-16-bit
PHR: BC-24-bit
PHR: CC-32-bit
PHR: BCH-16-bit
word error rate (WER)
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
-16
-14
-12
-10
-8
-6
$10\log_{10}(\mathrm{SNR}_{chip})$ [dB]

Burst Errors: N_c consecutive chip values blanked out



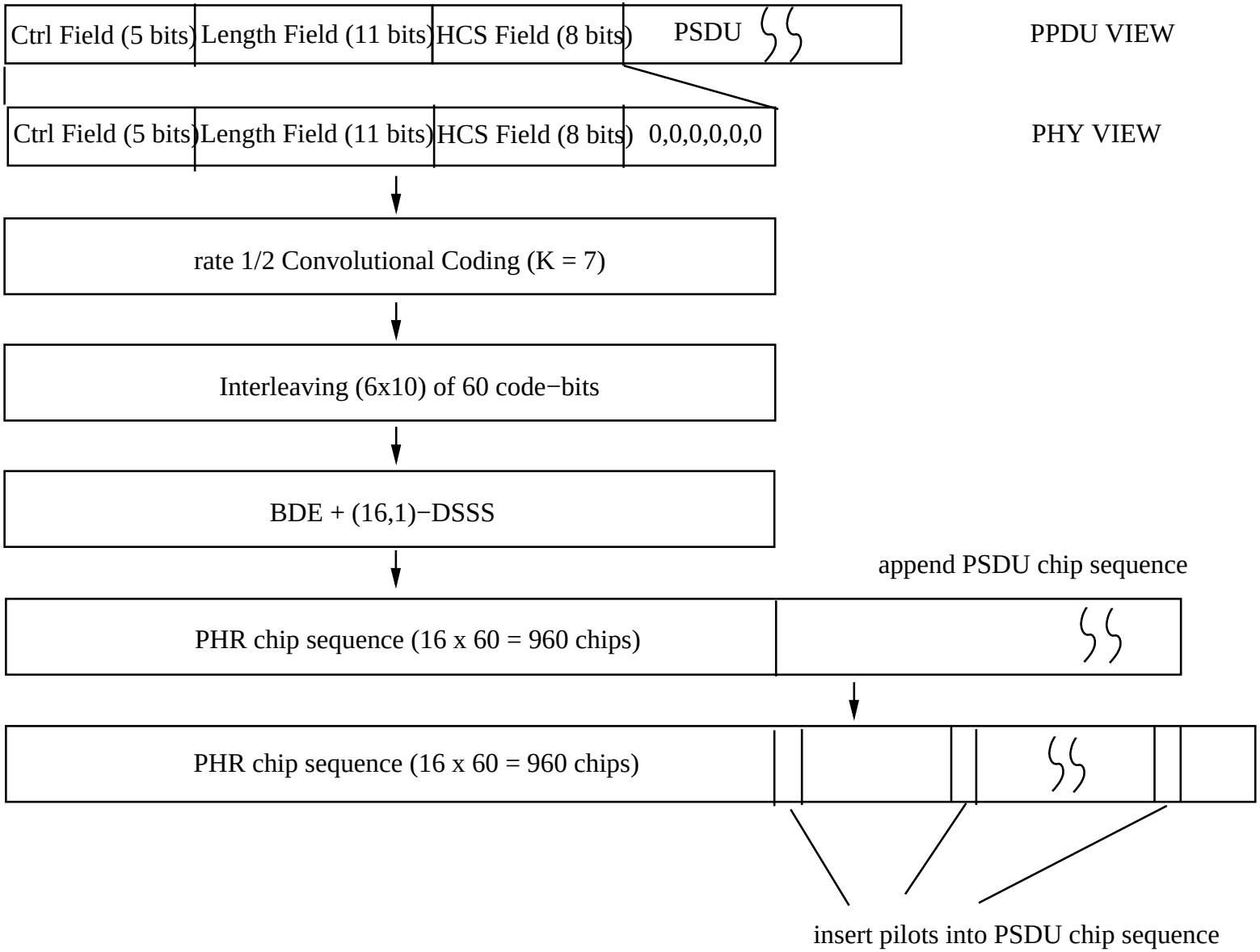
Issues related to BC-24-bit:

- Inserting a CRC-8 based HCS causes more overhead compared to CC-32 (i.e. 1536 chip samples versus 1024 chip samples).

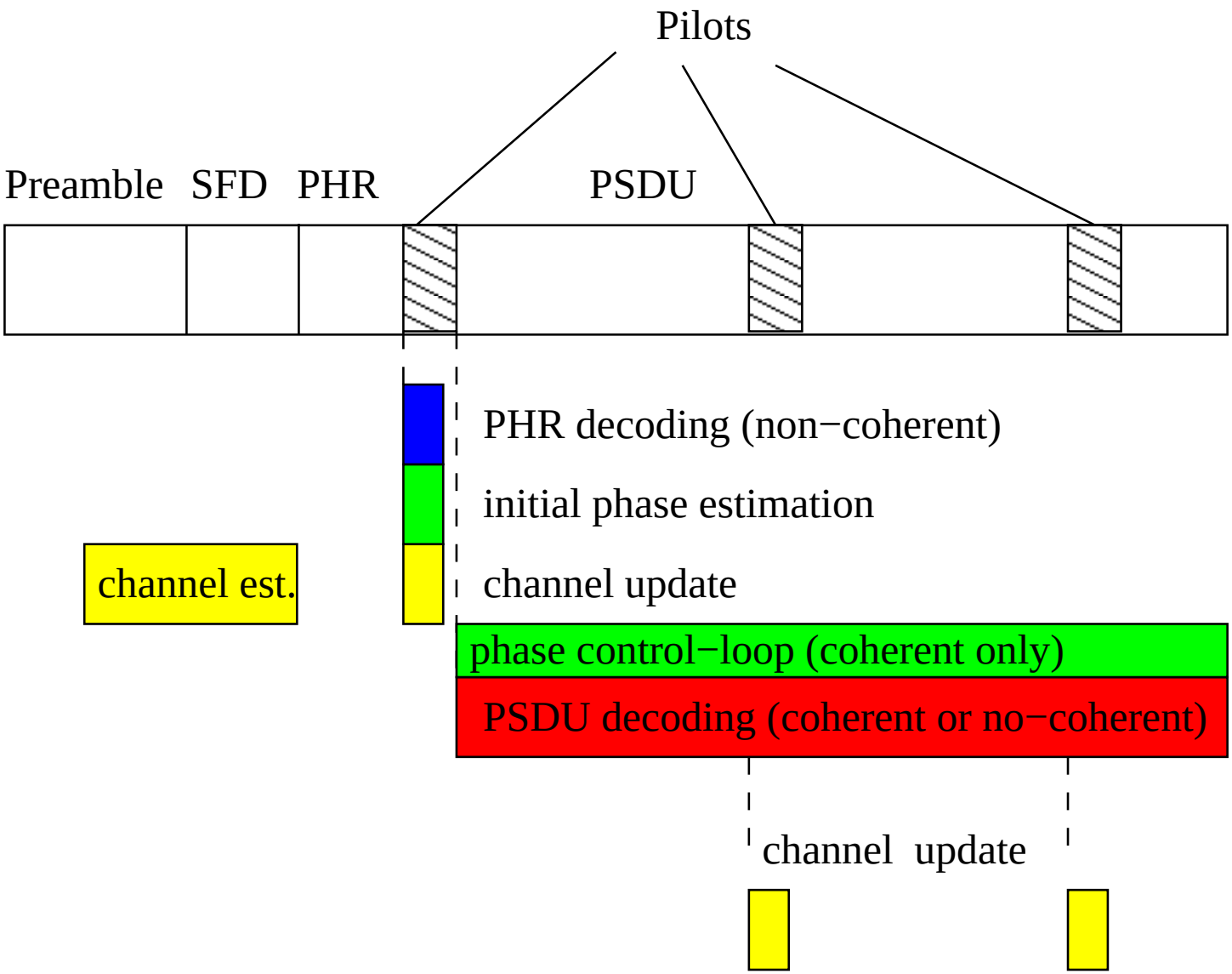
Issues related to CC-32-bit and BCH-16-bit:

- In contrast to the (32,8,13) code (processing data octet by octet), it is not possible to access reliable information of the Control field before all chip samples belonging to the PHR field are received.
- Consequently, chip samples belonging to the PSDU part need to be buffered while decoding the PHR field.
- The buffer size depends on the processing delay of the PHR FEC decoder.

CC-24-bit: Rate 1/2 Convolutional Coding with $K = 7$



Pilot symbols



Pilot symbols

- first pilot:
  - breathing space for PHR-FEC decoding
  - simplifies initial phase estimation[10]
  - simplifies initial channel estimation
- following pilots:
  - supports channel tracking for long packets when combined with equalization (500 kbit/s PSDU data rate)
  - supports timing point tracking for long packets (all PSDU data rates)

[10] used for coherent detection of (N,4)-DSSS or (N,8)-MDSSS during PSDU

Candidates for pilot symbols (780 / 915 MHz band)

pilot length # chips	pilot duration [us]	inter pilot spacing # chips
32x4 = 128	128	2048
16x4 = 64	64	1024

- Assuming a 16-MHz processing clock, this implies 1024 and 2048 processing cycles, respectively.
- This keeps FEC decoder complexity at a moderate level.
- Pilot sequence shall support simple correlation based channel estimation.
- Reasonable inter pilot spacing with regard to expected coherence time while keeping data rate loss due to overhead small (approx. 6%)

PHR Error Detection

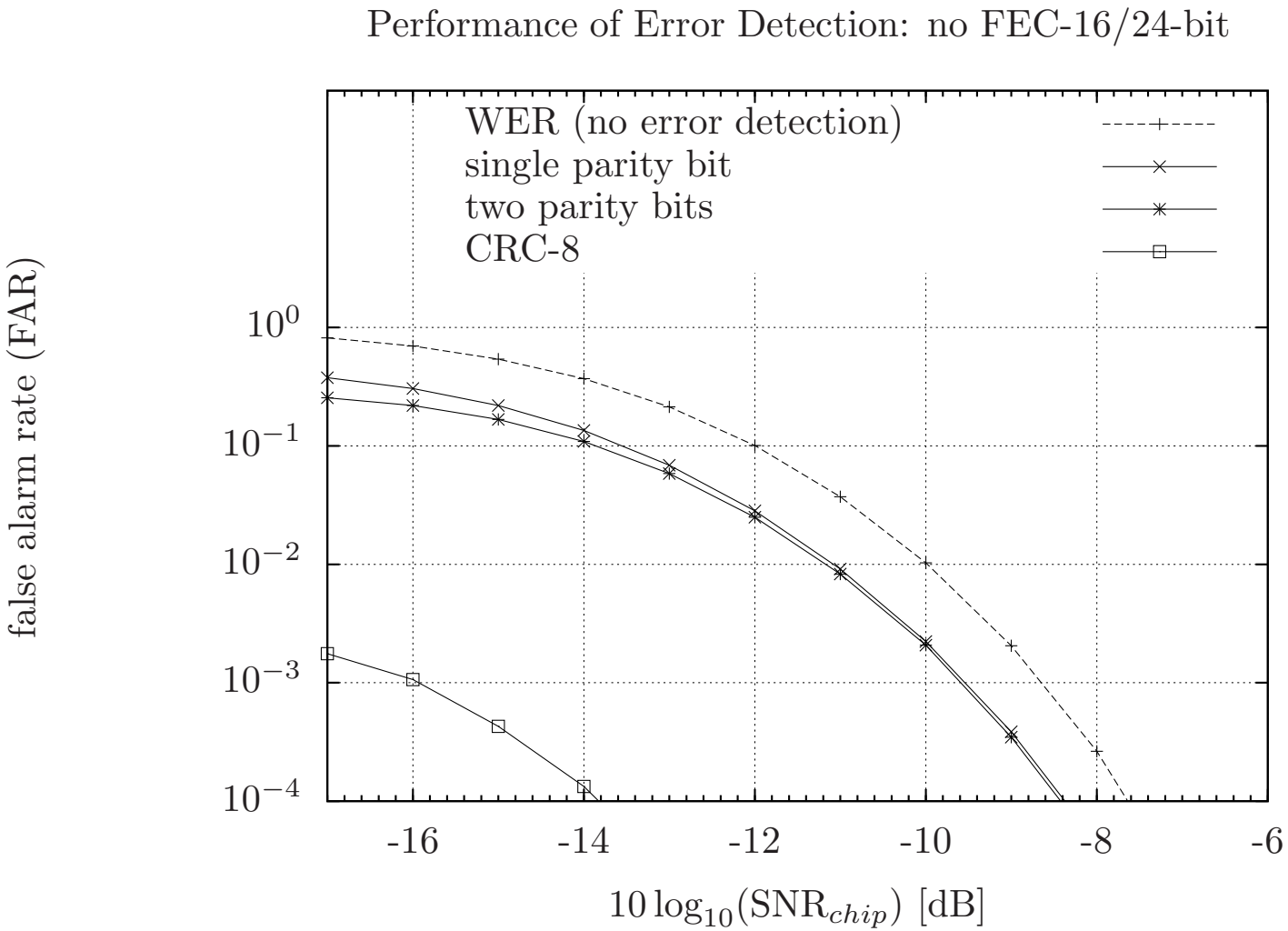
- reduces sync on frames with incorrectly decoded Ctrl or Length field information
- may cause overhead
- let E be the event a detected PHR field error
- let $\overline{E}\&\overline{A_0}$ be the event a non-detected PHR field error and the PHR Filed was incorrectly received
- let FAR (False Alarm Rate) denote the rate of occurrence of the event $\overline{E}\&\overline{A_0}$
- clearly, FAR = WER if no Error detection capability can be exploited

Candidates for PHR Error Detection

- single parity check bit PHR(0) over PHR(1:15)
- two parity check bits[11] PHR(0:1) over PHR(2:8) and PHR (9:15), respectively
- CRC-8 based HCS[12] with generator polynomial $X^8 + X^2 + X + 1$
- implicitly for BCH code (syndrome check)

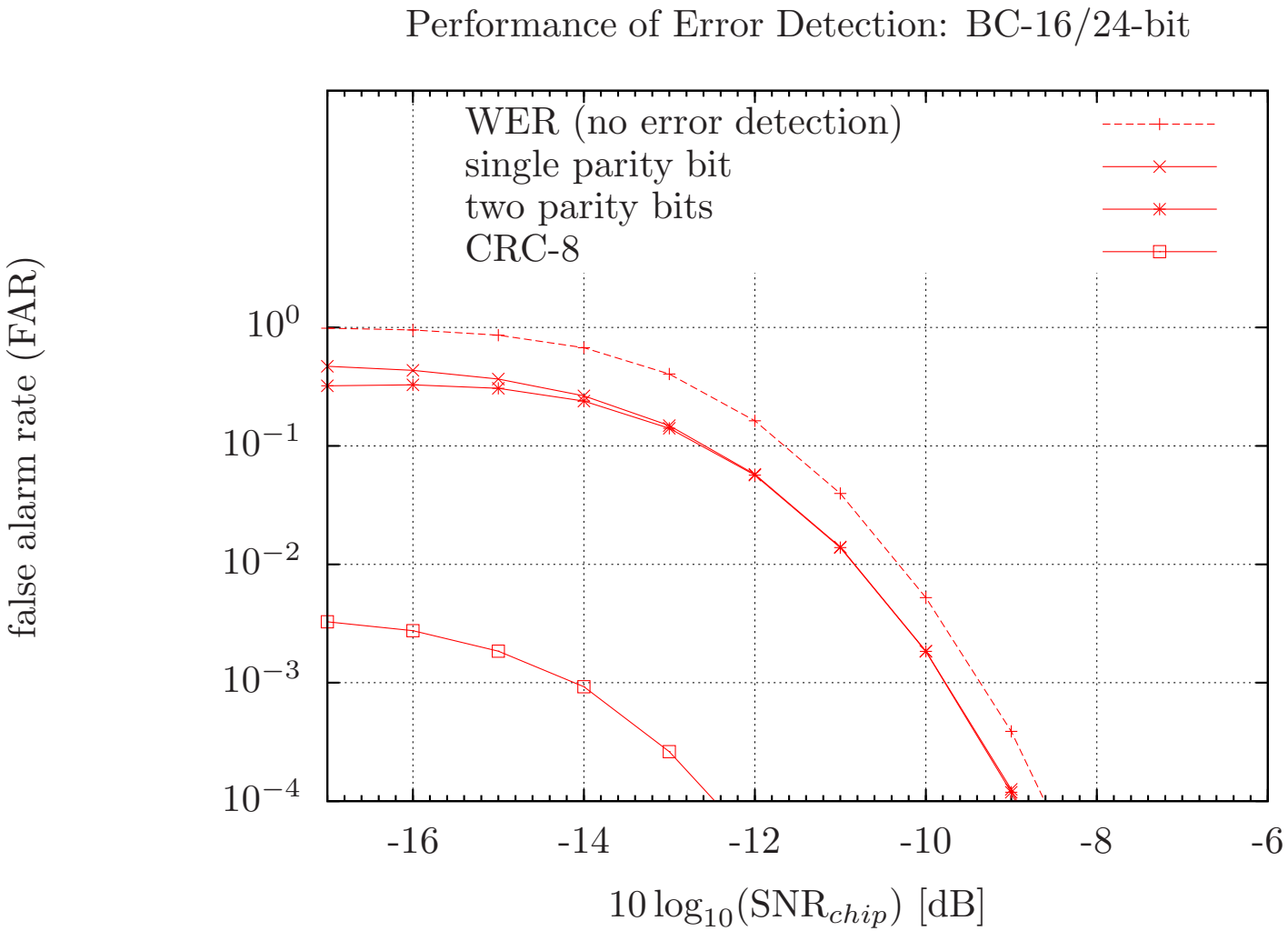
[11] as specified for the MR-O-QPSK PHY in draft P802.15.4g/d1,March 2010

[12] similar to the OFDM PHY in draft P802.15.4g/d1,March 2010



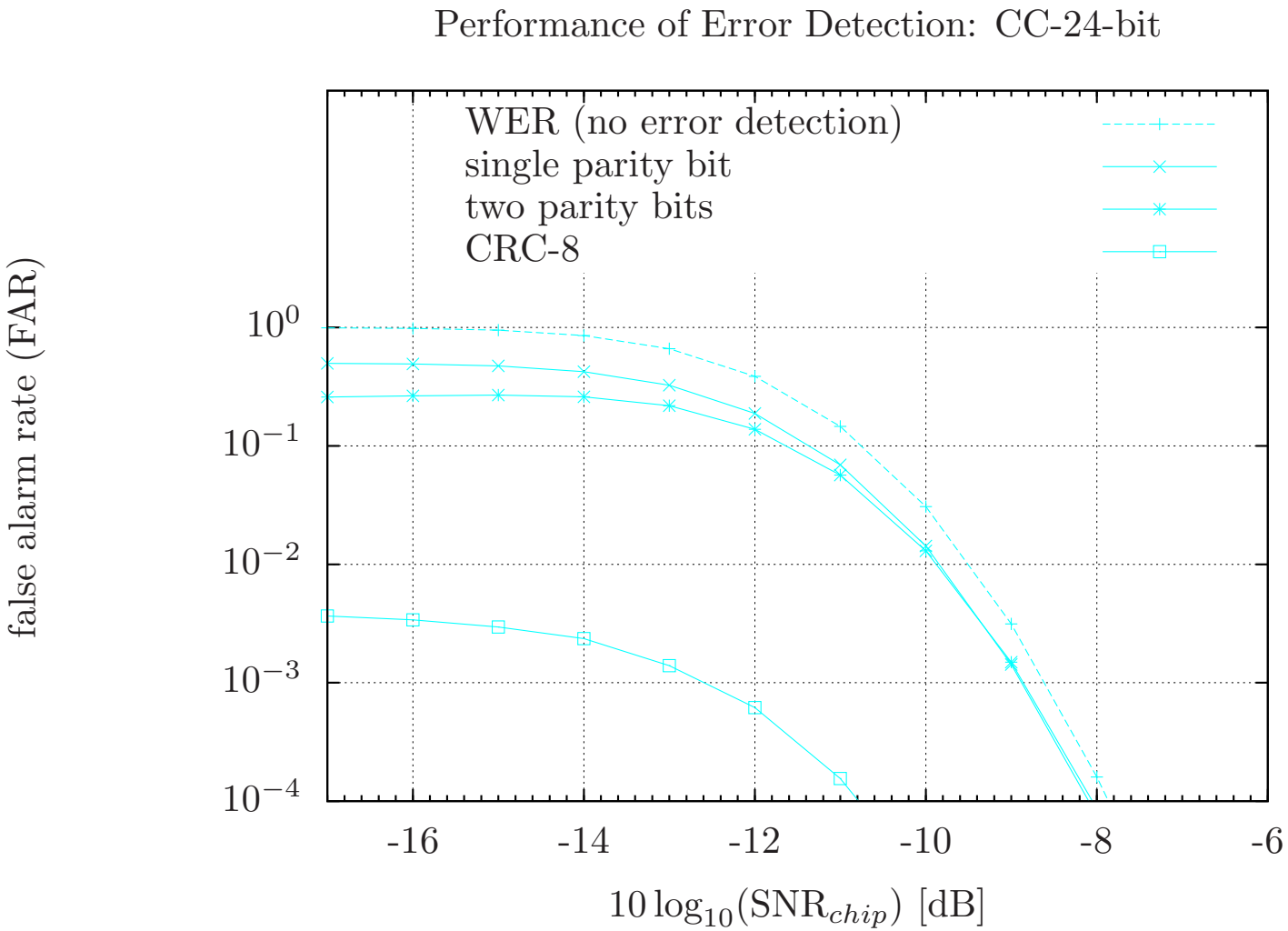
Two parity check bits: poor

CRC-8: good



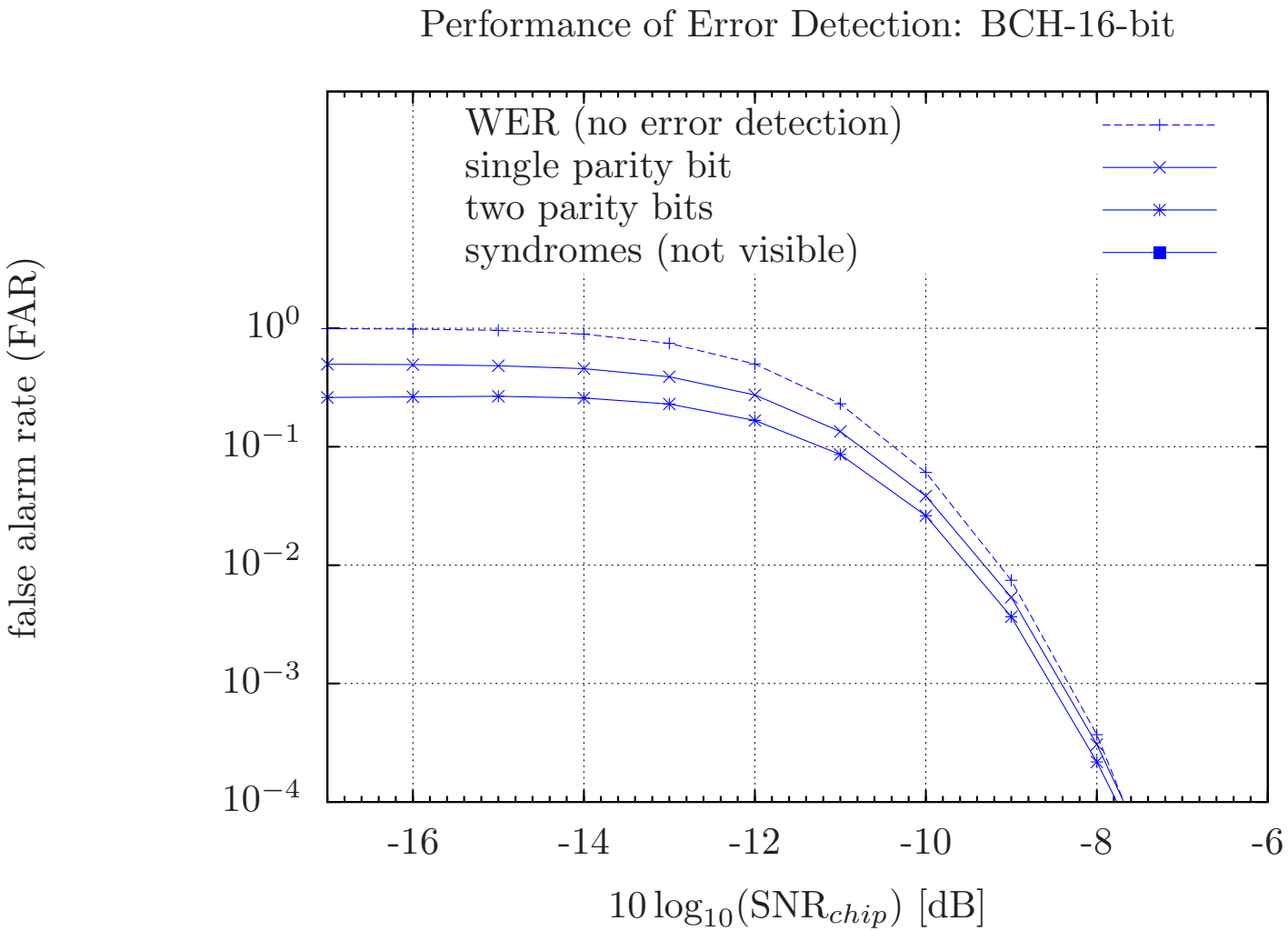
Two parity check bits: poor

CRC-8: good



Two parity check bits: poor

CRC-8: good



Two parity check bits: poor

Syndromes: nearly perfect[13]

[13] The BCH-(63,16,t = 11) code has a generator polynomial of degree 47.

Scheme	advantage	disadvantage
No-FEC-16-bit	▶ simple detection ▶ early access to Ctrl field (bit-by-bit)	▶ detection prone to frequency estimation and burst errors ▶ poor error detection (two parity bits)
No-FEC-24-bit	▶ simple detection ▶ early access to Ctrl field (bit-by-bit) ▶ good error detection (CRC-8)	▶ detection prone to frequency estimation and burst errors ▶ error detection: CRC-8 causes more overhead

Scheme	advantage	disadvantage
BC-16-bit	▶ robust detection ▶ early access to Ctrl field (octet by octet) ▶ simple decoder	▶ poor error detection (two parity bits)
BC-24-bit	▶ robust detection ▶ good error detection (CRC-8) ▶ early access to Ctrl field (octet-by-octet) ▶ simple decoder	▶ error detection: CRC-8 causes more overhead

Scheme	advantage	disadvantage
CC-24/32-bit	▶ very robust detection ▶ complex hardware of PSDU FEC decoder can be reused ▶ good error detection (CRC-8)	▶ late access to Ctrl field ▶ PSDU chip buffering required (unless pilots are prepended)
BCH-16-bit	▶ detection: sufficiently robust ▶ error detection: nearly perfect (syndromes) ▶ syndrome computation can already be performed during receive	▶ late access to Ctrl field ▶ additional complex hardware for FEC decoder required ▶ PSDU chip buffering required (unless pilots are prepended)

Conclusions

- PHR processing based on pure spreading without FEC is prone to frequency estimation errors and burst errors.

  PHR FEC is highly recommended!

- In order to benefit from PHR FEC, the uncoded SFD field should be extended 16 bits. This allows up to 3 SFD bit errors while keeping the false alarm rate low.
- Periodical insertion of pilots to the PSDU part is very useful for phase estimation, tracking and equalization. Decoding complexity of PHR FEC can be relaxed when prepending a first pilot sequences at the beginning of the PSDU part.
- PHR error detection based on 1 or 2 parity check bits is insufficient, especially in conjunction with FEC.