Project: IEEE P802.15 Working Group for Wireless Personal Area Networks (WPANs)

Submission Title: [The Low-cost RF-CMOS 60-GHz Transceiver]
Date Submitted: [13 March, 2007]
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Re: []

Abstract: [Description of the low-cost of RF-CMOS RFIC development]
Purpose: [Contribution to TG3c at March 2007 meeting.]

The Low-Cost RF-CMOS 60-GHz Transceiver

Tian-Wei Huang, Chi-Hsueh Wang, Hong-Yeh Chang*, Pei-Si Wu, Kun-You Lin, Jeng-Han Tsai, Chin-Shen Lin, Huei Wang, and Chun Hsiung Chen

National Taiwan University

***National Central University**

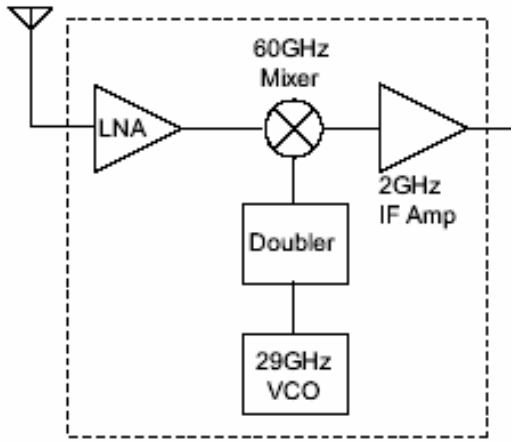
March 13, 2007

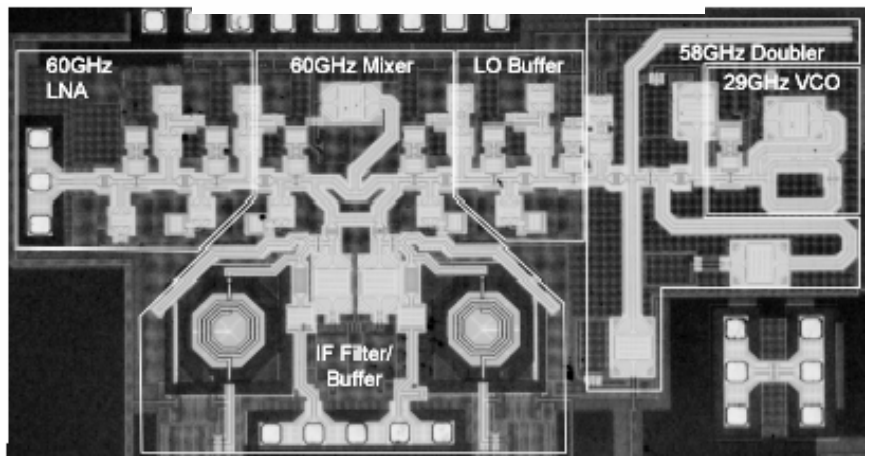
Agenda

- CMOS Low-power Transceiver
  - Low-power Tx
  - Low-power Rx
- CMOS Active Mixer

Publication Review (60-GHz Rx)

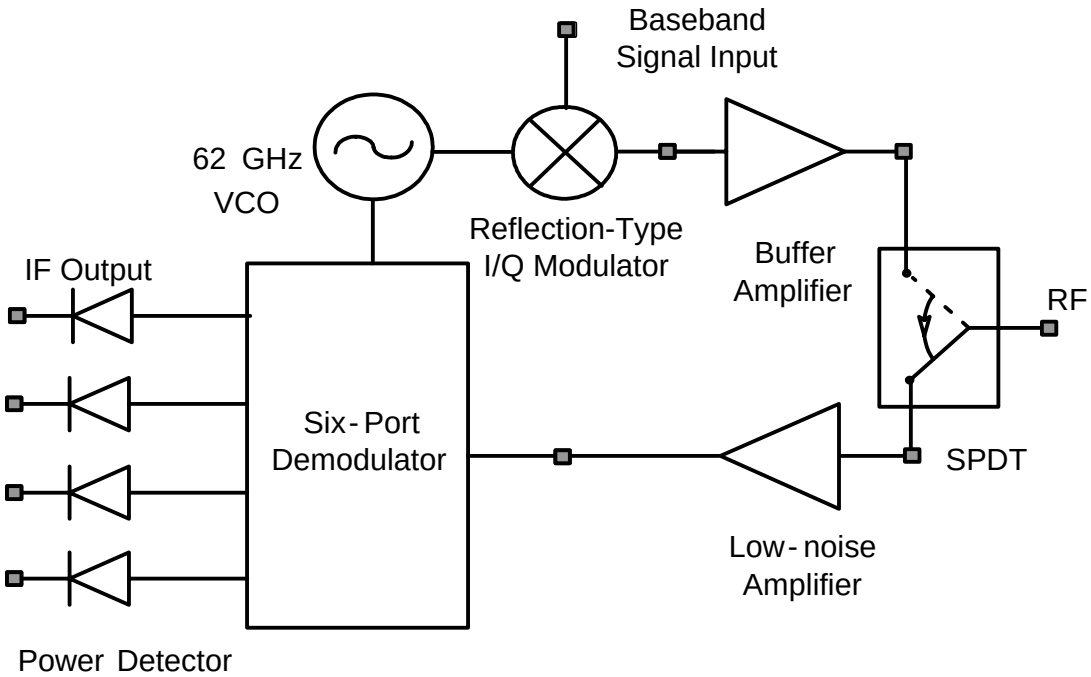
- Technology: 0.13 μm CMOS technology
- Chip size: 3.8 mm^2
- VCO+Doubler: +2dBm@59GHz,
  -86dBc/Hz@1MHz offset
- Mixer: CG > -2dB@60GHz, P_{LO}=0dBm
- DC power consumption: 77mW

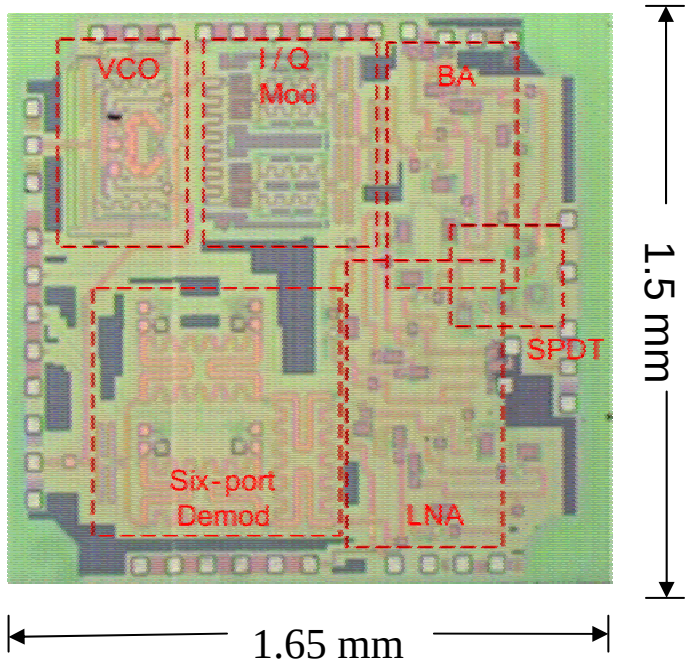




Sohrab Emami, Chinh H. Doan, Ali M. Niknejad, and Robert W. Brodersen,"A Highly Integrated 60GHz CMOS Front-End Receiver," 2007 *International Solid-State Circuit Conference (ISSCC),* San Francisco, CA, Feb. 2007.

The Low-power Transceiver Structure

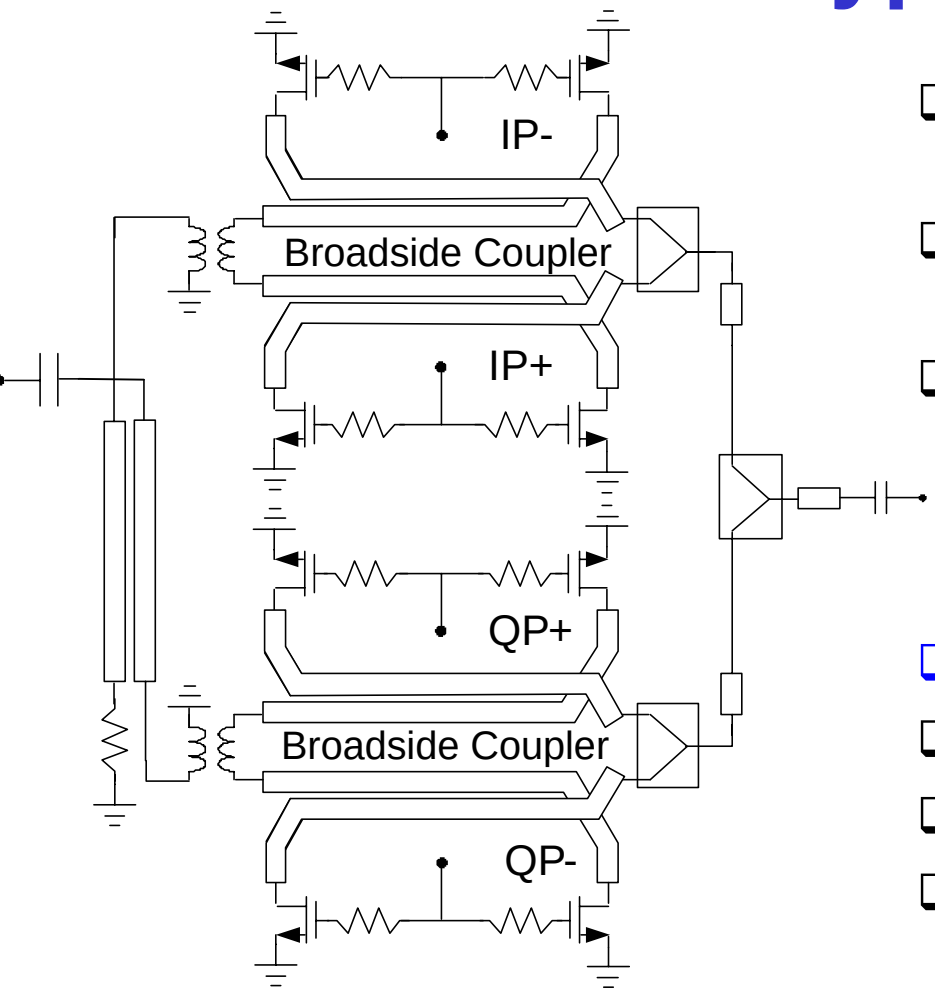




- 0.13 μm CMOS, Low power consumption, and Low LO power
- Miniature chip size, and **Low Cost**

C-H. Wang, H-Y. Chang, P-S. Wu, K-Y. Lin, T-W. Huang, H. Wang, C-H. Chen, "A 60GHz Low-Power Six-Port Transceiver for Gigabit Software-Defined Transceiver Applications," 2007 *International Solid-State Circuit Conference (ISSCC),* San Francisco, CA, Feb. 2007.

Reflection-Type I/Q Modulator



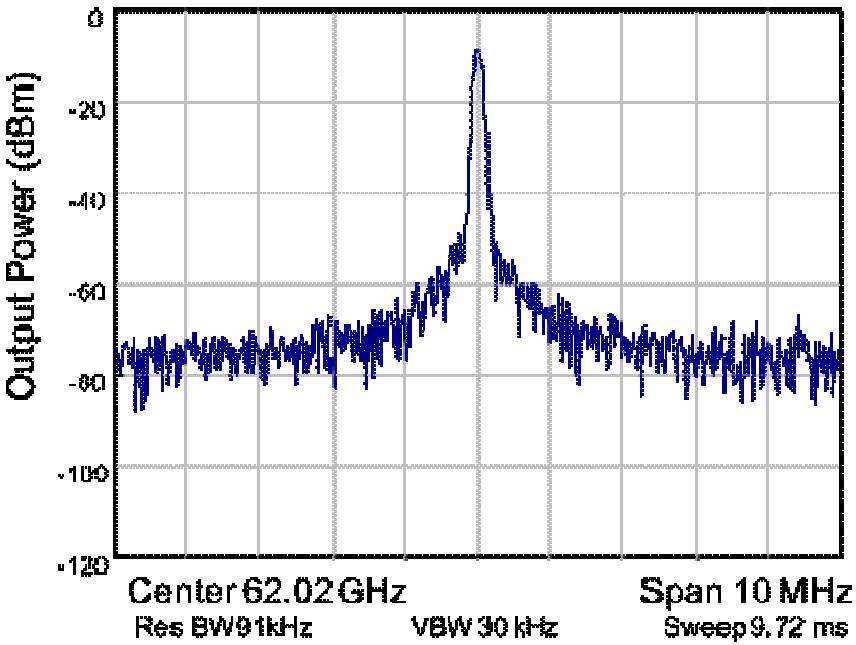
- Meandered broadside coupler to implement 90 ° hybrids.
- Marchand-type transformer to implement the 180 ° hybrid.
- Wilkinson power combiner for in-phase combiner

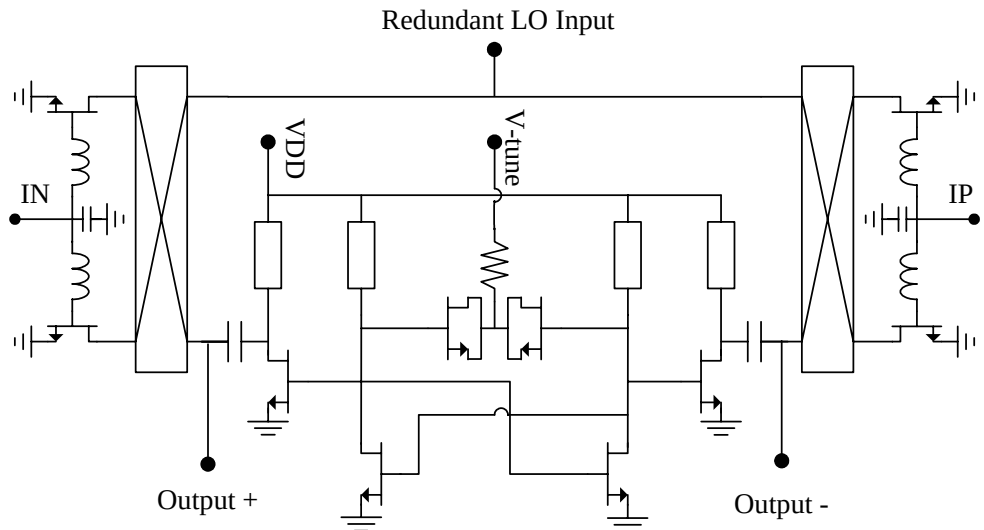
- **Low LO drive power**
- Low DC power consumption
- High linearity, broad Bandwidth
- I/Q modulation

Hong-Yeh Chang, and et al, "Design and analysis of CMOS broad-band compact high-linearity modulators for gigabit microwave/millimeter-wave applications," *IEEE Transactions on Microwave Theory and Techniques*, Jan. 2006.

VCO Design and Testing

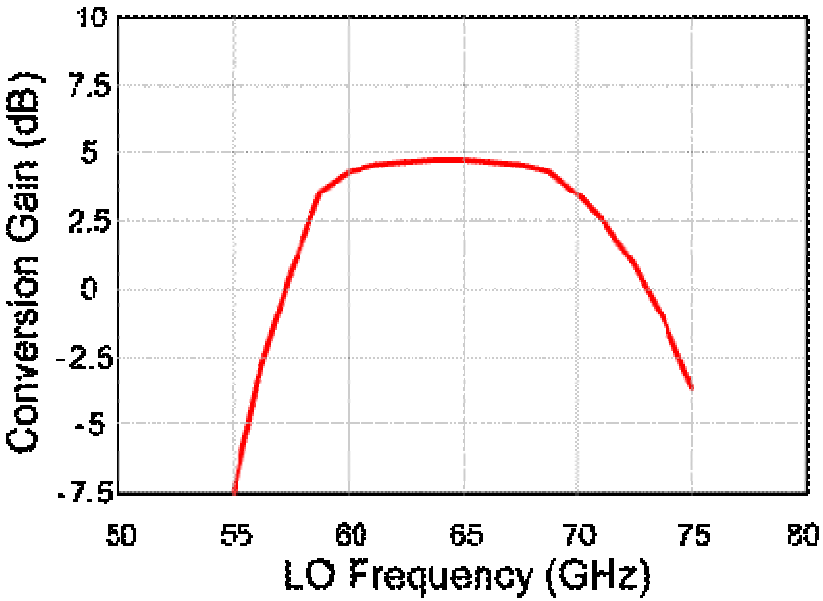
Measured Output Spectrum



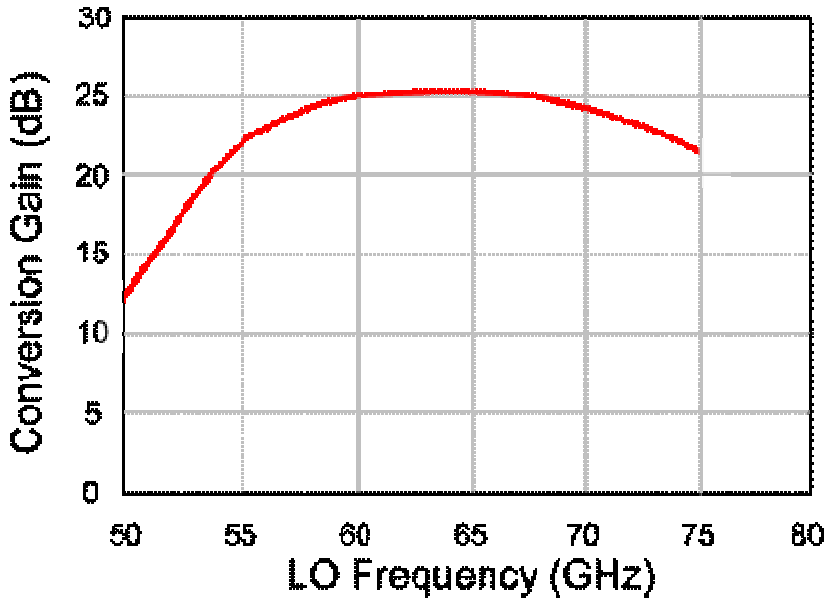


- Phase noise: -92.2 dBc/Hz @ 1MHz offset at 62 GHz
- Output power at the test port: -12.1 dBm

Measured Transmitter Conversion Gain



Low Gain Mode

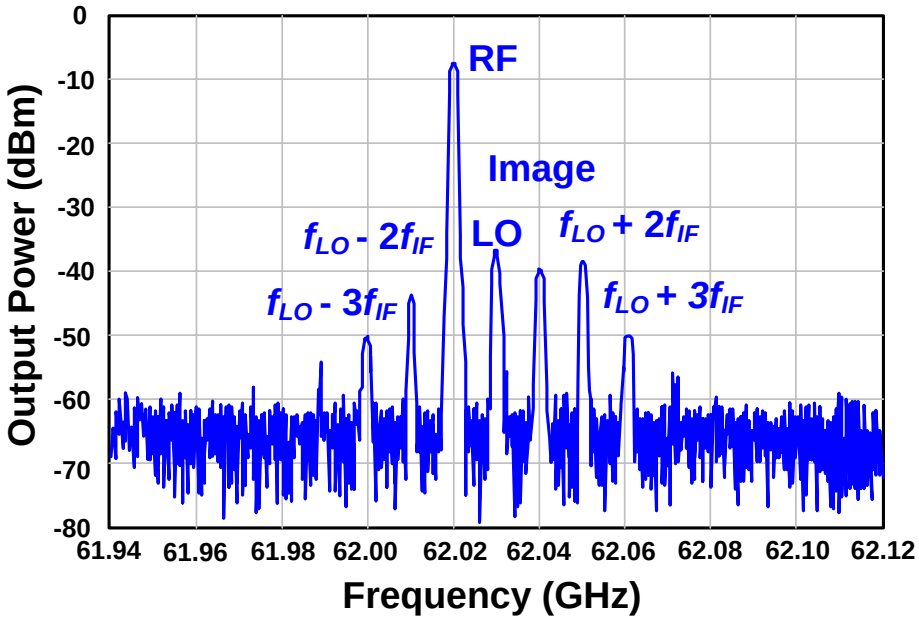


High Gain Mode

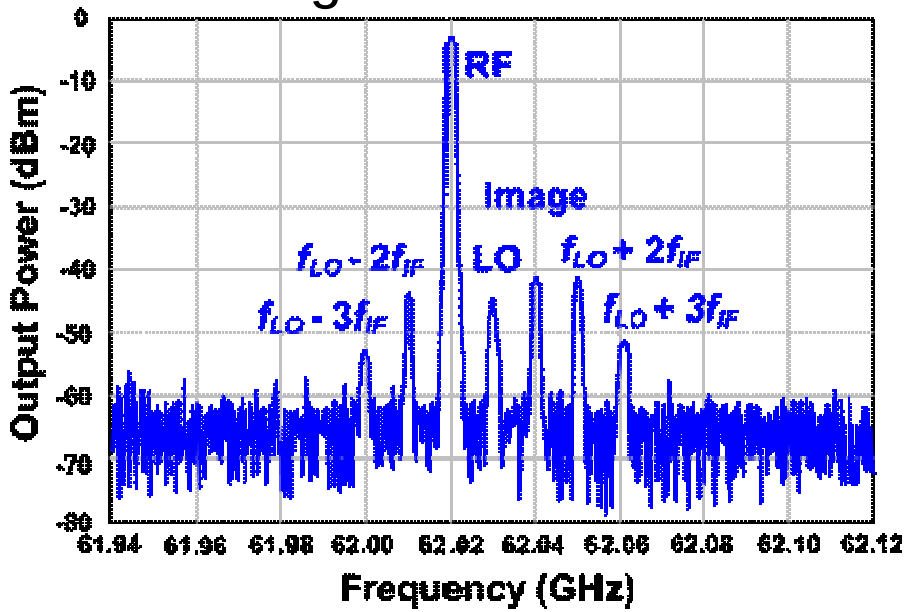
- Conversion gain : 4-5dB at low gain mode, (60-68 GHz)
- Conversion gain : 24-25dB at high gain mode, (57-70 GHz)
- DC power consumption : 36.9 mW at low gain mode
  72 mW at high gain mode

Measured Output Spectrum for QPSK Signal

Low Gain Mode

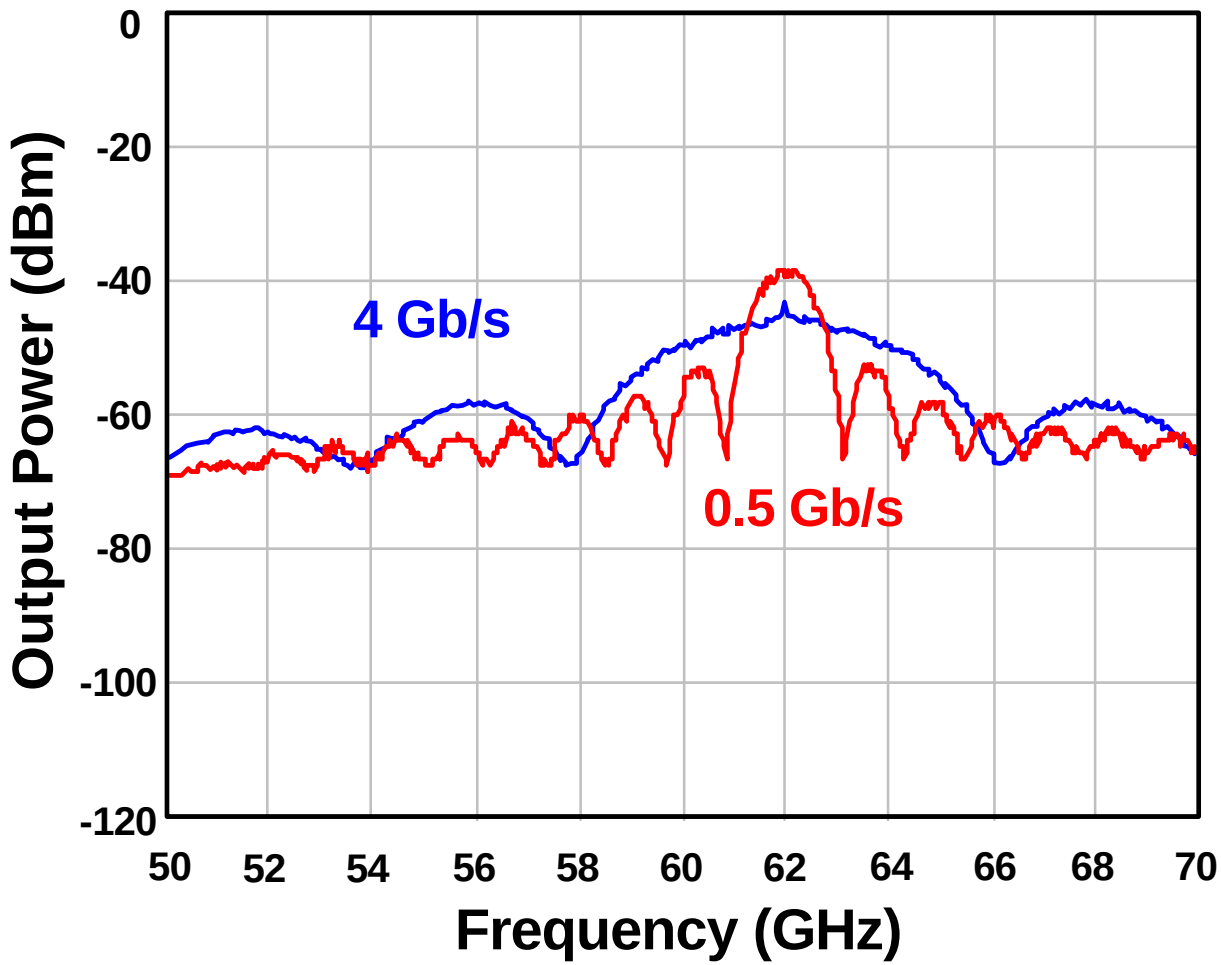


High Gain Mode



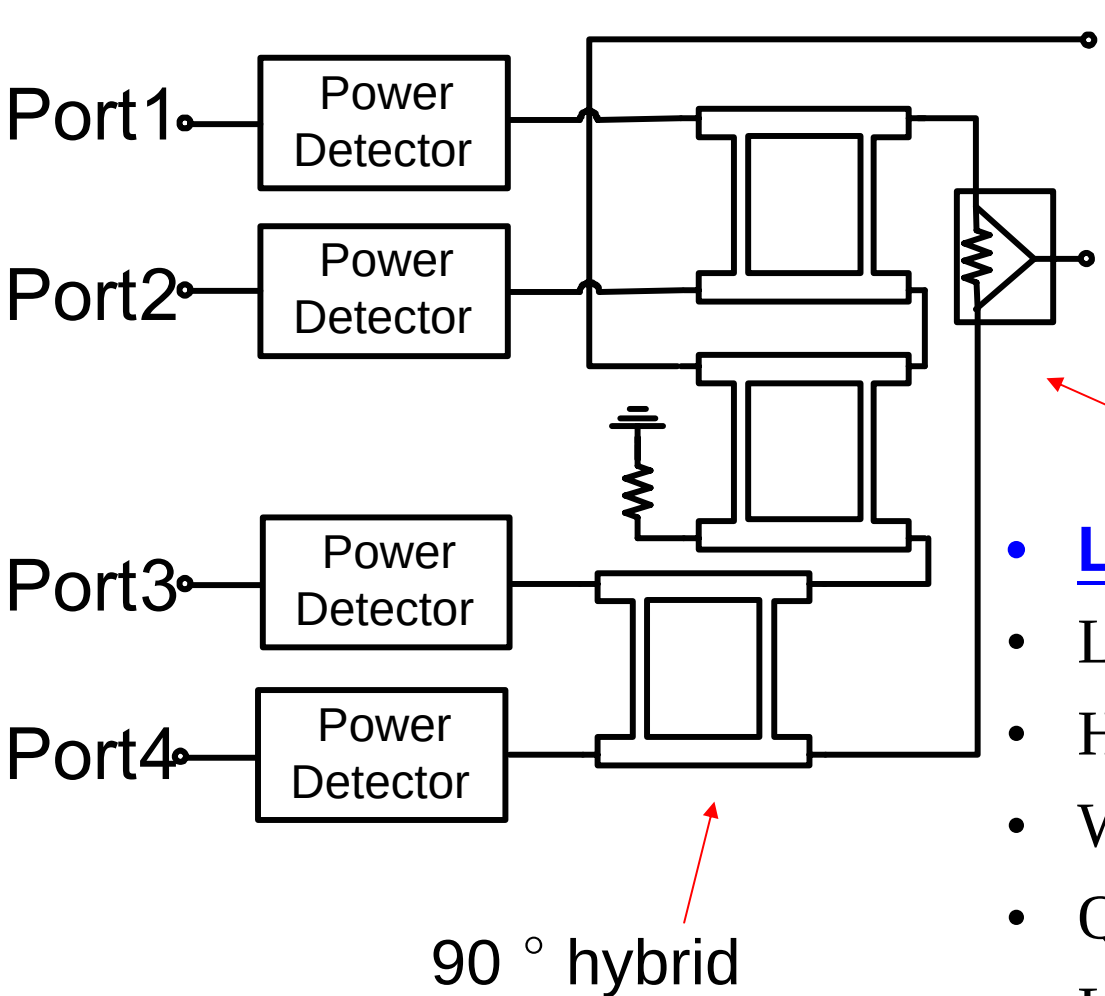
- Low gain mode : Image suppression> 30 dBc,
  LO suppression> 20 dBc, $f_{LO} \pm 2f_{IF}$ > 30 dBc,
  $f_{LO} \pm 3f_{IF}$ > 40 dBc, (60 to 64 GHz)
- High gain mode : Image suppression> 35 dBc,
  LO suppression> 30 dBc, $f_{LO} \pm 2f_{IF}$ > 35 dBc,
  $f_{LO} \pm 3f_{IF}$ > 40 dBc, (60 to 64 GHz)

Measured Output Spectrum for BPSK Signal



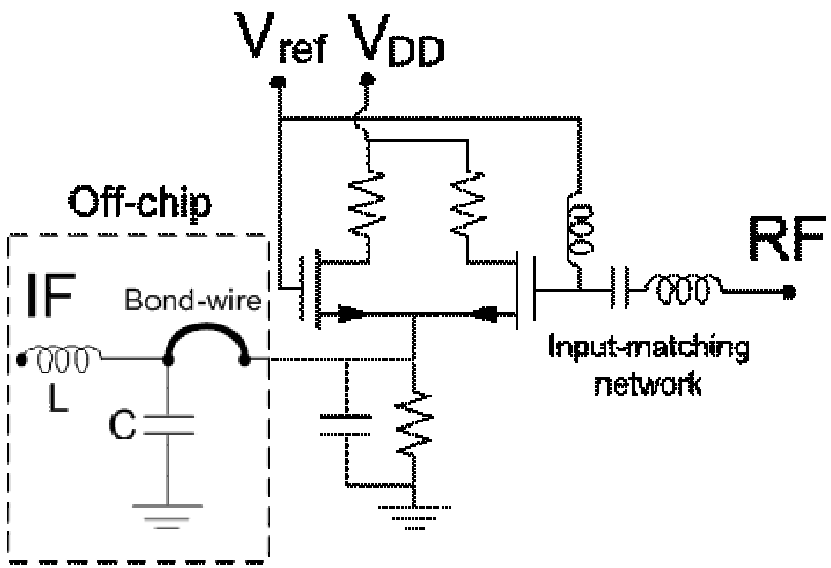
- Spectrum spread out due to unfiltered baseband signals

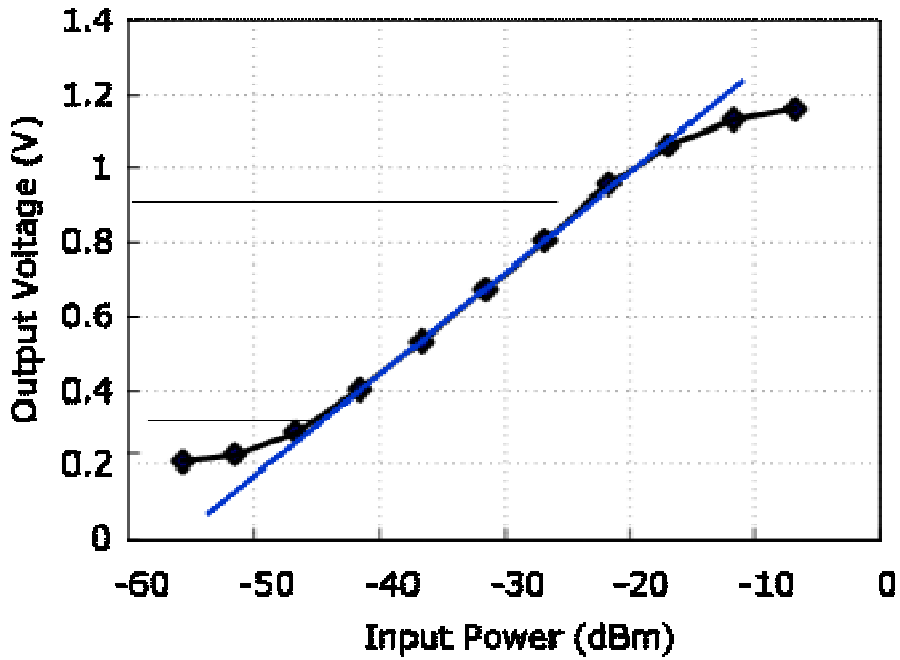
60 GHz Six-Port Reflectometer



- **Low LO drive power**
- Low DC power consumption
- High linearity
- Wide bandwidth
- QAM Modulation
- Low cost (for very high frequency)

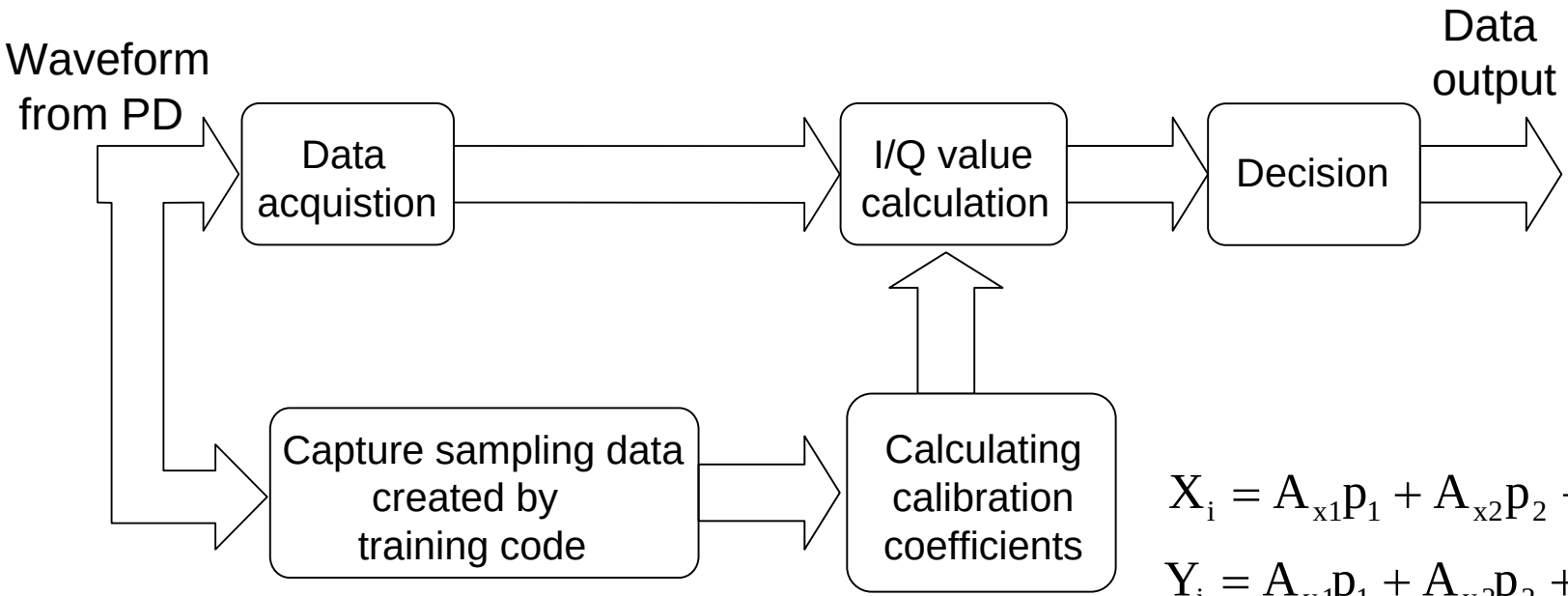
60 GHz Power Detector





- Input-matching network enhance sensitivity
- Sensitivity > 10000mV/mW (including LNA)
- V_{ref} set for maximum dynamic range
- Off-chip L and C values to achieve different modulation bandwidth

Real-Time Calibration Process

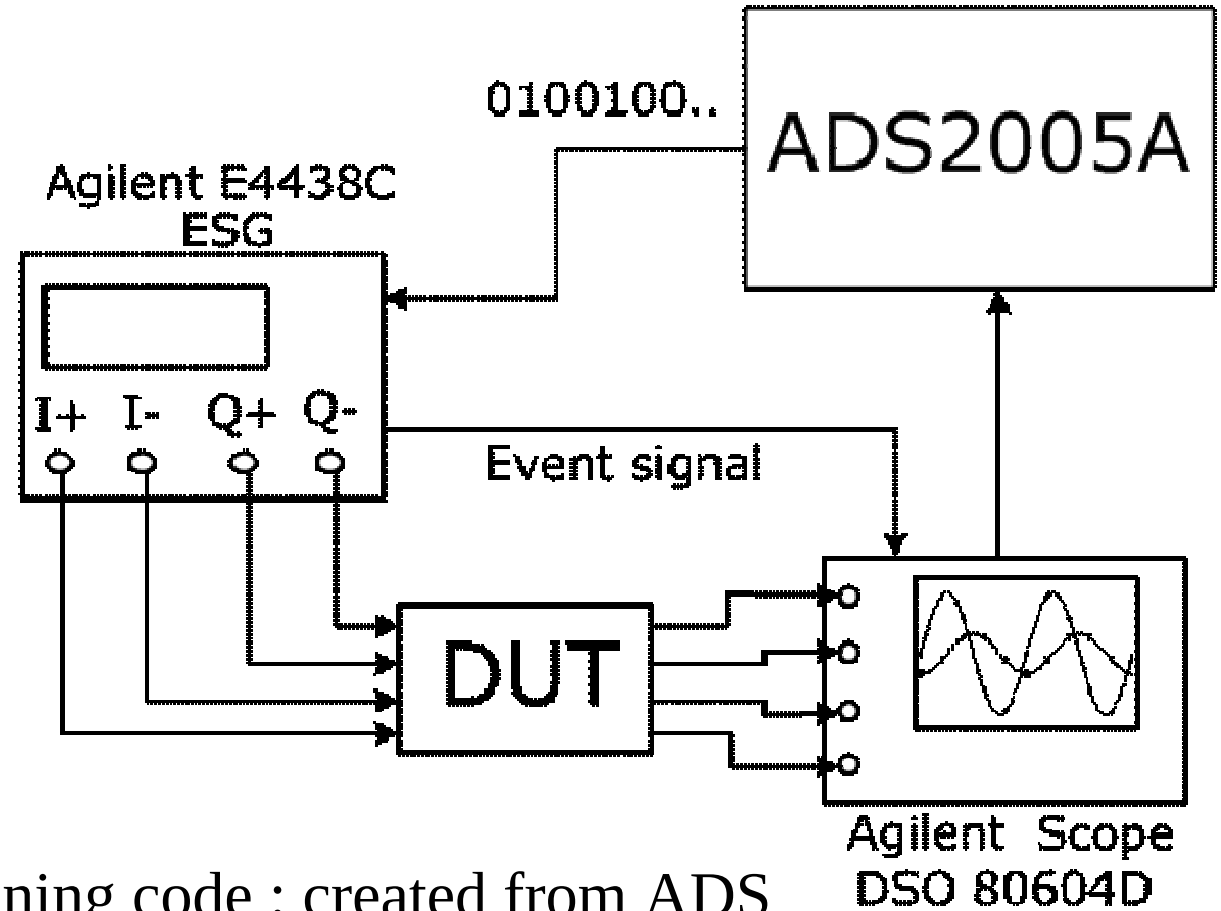


$$X_i = A_{x1}p_1 + A_{x2}p_2 + A_{x3}p_3 + C_x$$

$$Y_i = A_{y1}p_1 + A_{y2}p_2 + A_{y3}p_3 + C_y$$

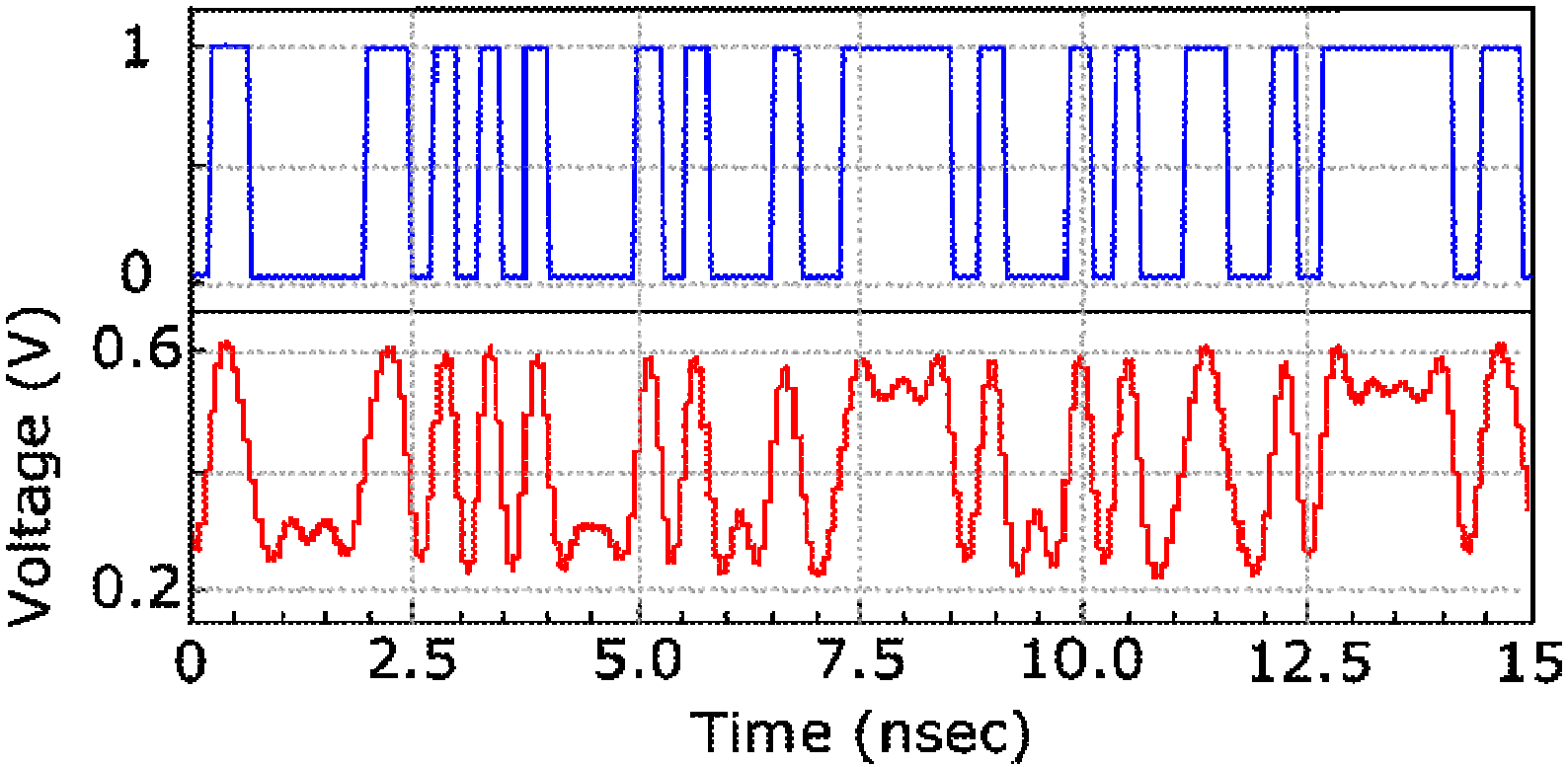
- X_i, Y_i : calculated output data
  A_{xi}, A_{yi}, C_x, C_y : calibration parameters to be determined
- p1, p2, p3 : power ratios at the output detectors
- Known training code : calculate A_{xi}, A_{yi}, C_x, and C_y
- Non-ideal effects eliminated after real-time calibration process

Measurement Setup



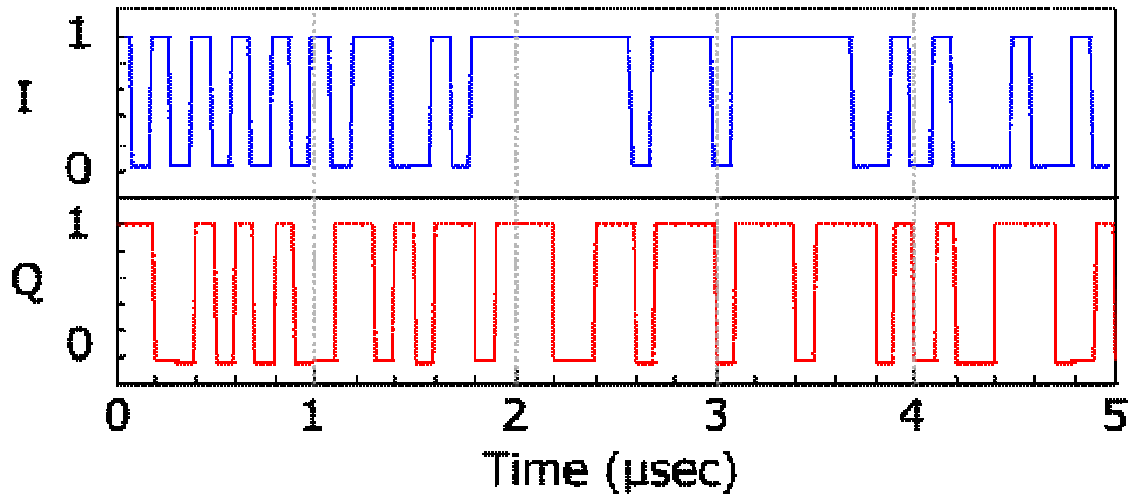
- Training code : created from ADS
- Capture waveform from real-time scope
- Instruments : controlled by ADS

Demodulation Results for BPSK Signal

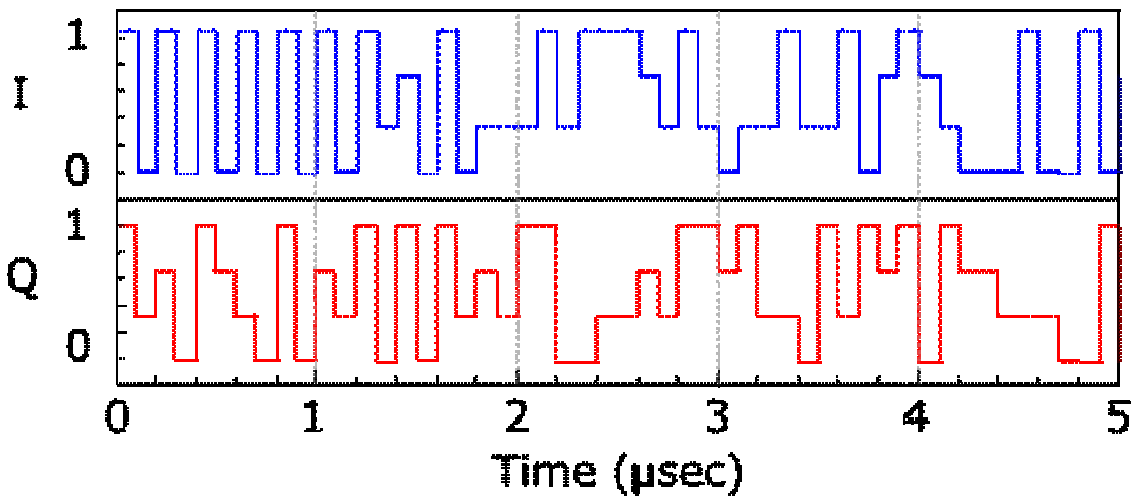


- Measured EVM of the 40Mb/s BPSK signal is lower than 4% with an input power of -30dB
- Data rate of BPSK modulation signals up to 4Gb/s

Demodulation Results for QPSK & 16QAM

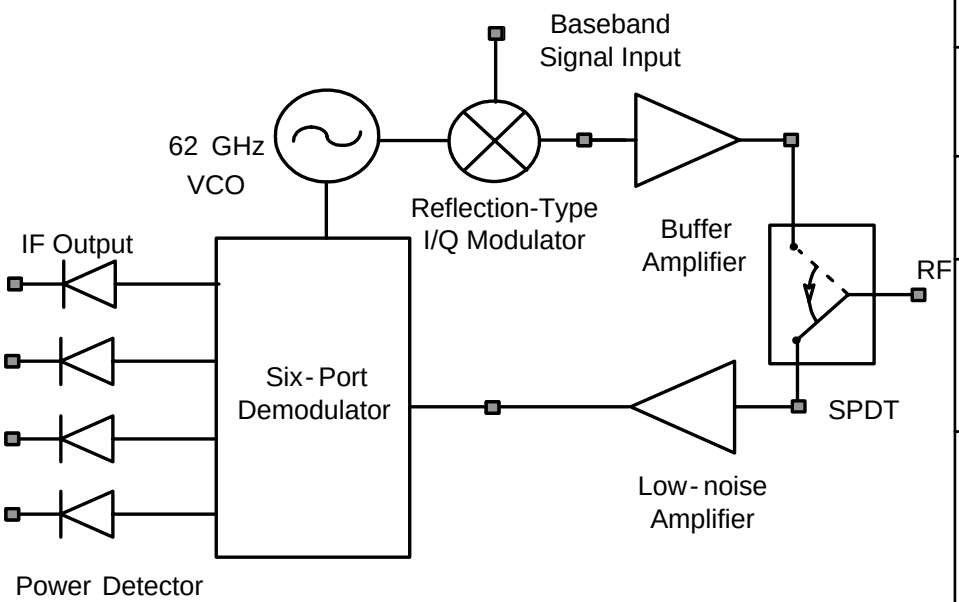


QPSK



16QAM

Performance Summary



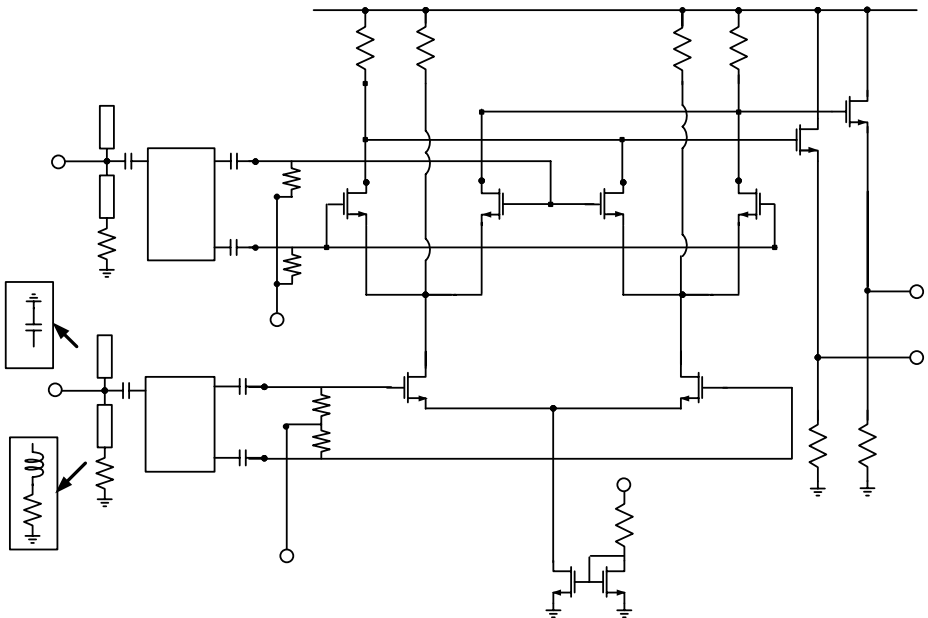
- Tx : Reflection-type modulator
- Rx: Six-port reflectometer

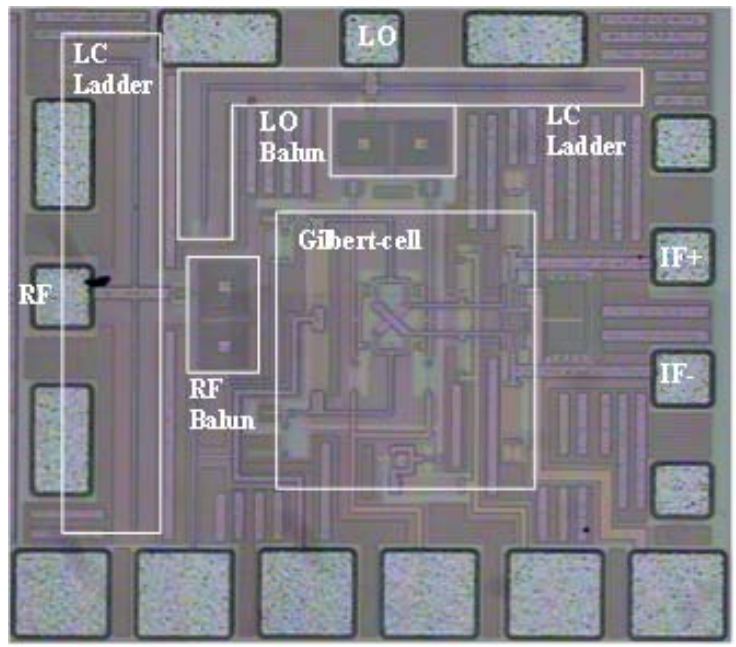
Performance Summary	
Frequency (GHz)	60 ~ 67
Tx P_{out} (dBm)	-2
Rx min P_{in} (dBm) (no IF Amp)	-50
Rx NF (dB) (Simulated)	10
Modulation	QAM
VCO P_{out} (dBm)	> -10
DC Power Consumption (mW)	~ 97.9

25-75 GHz 90nm CMOS Gilbert-cell Mixer

Process : 90nm CMOS
Topology : Gilbert-cell
Chip size: 0.55 mm ˟ 0.55 mm
RF Frequency : 25-75 GHz

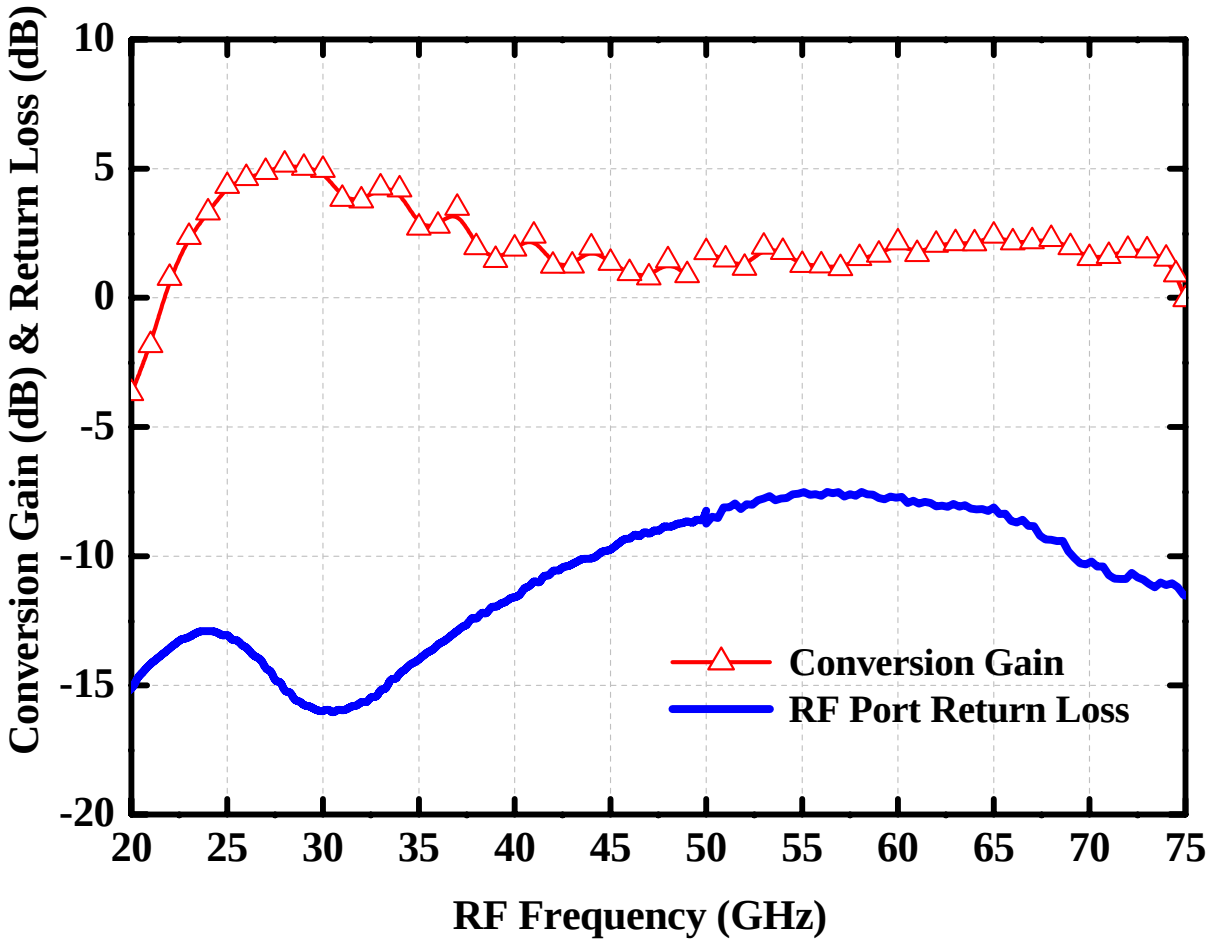
Conversion Gain : 3 ± 2 dB
LO Driver Power : 6 dBm
Power Consumption : 93 mW
Isolation : 30 dB



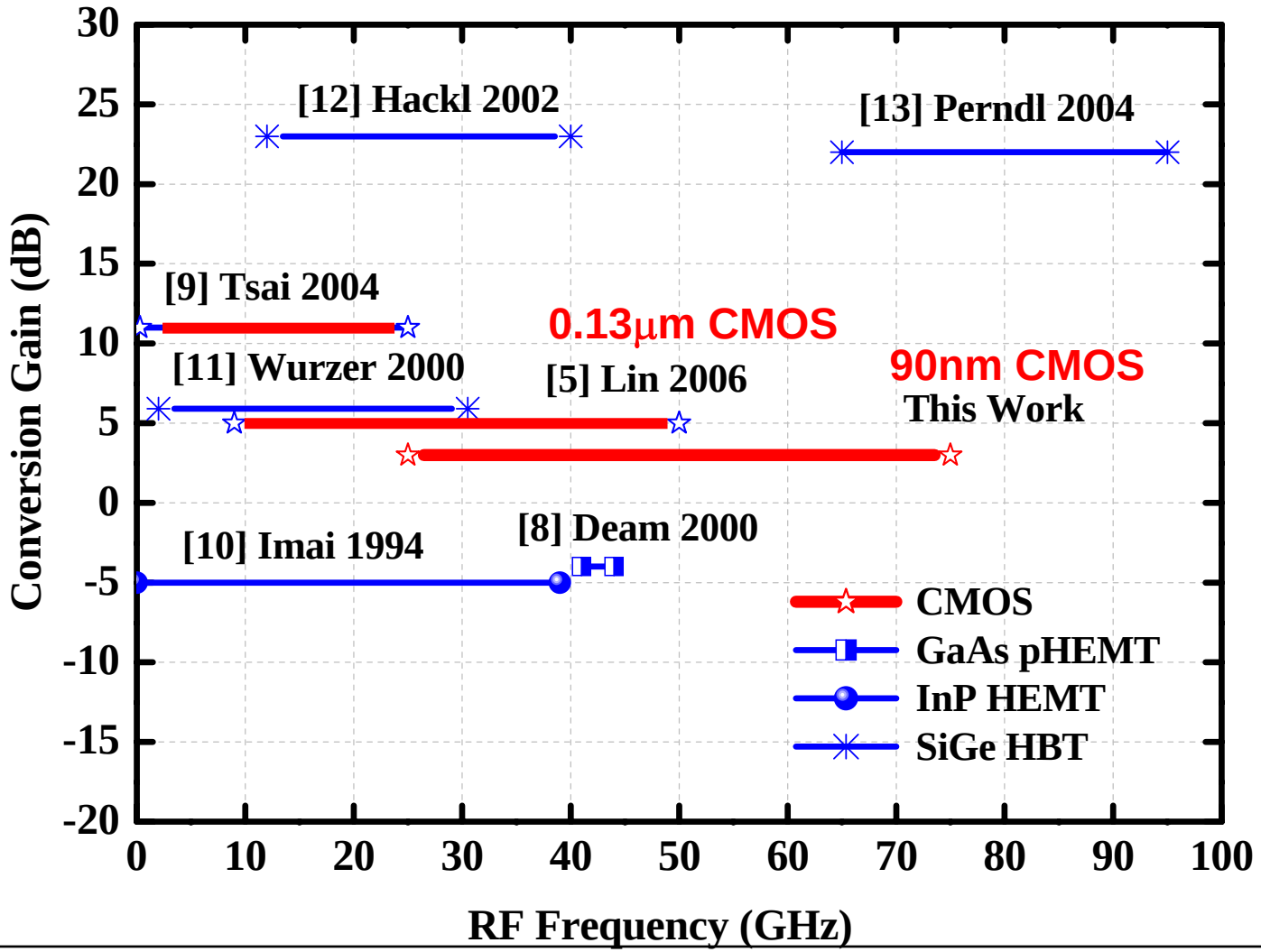


Jeng-Han Tsai, Pei-Si Wu, Chin-Shen Lin, Tian-Wei Huang, John G.J. Chern, and Wen-Chu Huang, " A 25-75-GHz Broadband Gilbert-cell Mixer Using 90-nm CMOS Technology," accepted by *IEEE Microwave and Guided Wave Letters*, April 2007.

Measurement Results



Conversion Gain and BW Comparison



LO Power and Chip Size Comparison

Process	Design Topology	Bandwidth (GHz)	Conversion Gain (dB)	LO Power (dBm)	Chip Size (mm2)	Ref.
GaAs pHEMT	Fundamental Gilbert Cell	41-44	-4	0	1.7	[8]
GaAs pHEMT	Subharminic Resistive Gate-Pumped	39-48	-12.5 ± 1.5	5	0.72	2007 APMC
90-nm SOI CMOS	Fundamental Resistive Gate-Pumped	26.5-30	-10.3	0	0.121	2005 /08 TMTT
0.13-μm CMOS	Fundamental Resistive Gate-Pumped	~ 60	-2	0	n/a	2007 ISSCC
0.13-μm CMOS	Fundamental Gilbert Cell	9 - 50	+5	5	0.25	[5]
90-nm CMOS	Fundamental Gilbert Cell	25 - 75	+3 (±2)	6	0.3	This Work

Summary

- Presented a 60-GHz six-port transceiver IC in standard-bulk 0.13μm CMOS technology.
- Presented a 25-75 GHz Gilbert-cell mixer in standard-bulk 90nm CMOS technology.
- 60-GHz LO power level in 0.13μm CMOS is a key factor for chip size and cost.

Thank you!