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Wireless Personal Area Networks

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Abstract	[Detailed information for the MERGED PROPOSAL #2. The summary detail is contained in document 04/xxxx.]
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DS-UWB Physical Layer Submission to 802.15 Task Group 3a

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1 PHY specification for Ultra-Wideband

1.1 Introduction

This clause specifies the PHY entity for an ultra-wideband (UWB) system that utilizes the unlicensed 3.1 – 10.6 GHz UWB band, as regulated in the United States by the Code of Federal Regulations, Title 47, Section 15.

The UWB system provides a wireless PAN with data payload communication capabilities of 28, 55, 110, 220, 500, 660 and 1320 Mbps. The proposed UWB system employs direct sequence spreading of a binary phase shift keyed UWB pulses. Forward error correction coding (convolutional coding) is used with a coding rate of ½ and ¾. The proposed UWB system also supports operation in two different bands: one band nominally occupying the spectrum from 3.1 to 4.85 GHz (the low band), and the second band occupying the spectrum from 6.2 to 9.7 GHz (the high band).

1.1.1 PHY Overview

1.1.1.1 The Direct Sequence UWB data modes

The DS-UWB PHY waveform is based upon dual-band bi-phase modulation with root raised cosine baseband data pulses. DS-UWB supports two independent bands of operation. The lower band occupies the spectrum from 3.1 GHz to 4.85 GHz and the upper band occupies the spectrum from 6.2 GHz to 9.7 GHz.

Within each band there is support for up to six piconet channels to have unique operating frequencies and acquisition codes. A compliant device is required to implement only support for piconets channels 1-4 in the low band. Support for piconets channels 5-12 is optional.

Binary phase shift keying is used to moduate the data sumbols, with each transmitted symbol being composes of a sequence of UWB pulses. The various data rates are supported through the use of variable-length spreading code sequences, with sequence lenghts ranging from 1 to 24 pulses or “chips”.

The PHY Header contains information which indicates the symbol rate, the number of bits per symbol and the FEC scheme used. From this information the DEV calculates the resulting bit rate.

The PHY preamble uses one of six available piconet access codes (PACs) for acquisition (corresponding to the piconet channel being used). The PNC selects the operating PAC during piconet establishment. There are 3 preamble lengths depending upon the application bit rate:

1. Short preamble: 10 uS in length that requires a high SNR with low channel dispersion - it is most suitable for high bit rate, short range links (<3 meters)

2. Nominal preamble: 15 uS in length that requires a nominal SNR with a nominal channel - it is the default preamble choice
3. Long preamble: 30 uS in length that is used for a poor SNR and/or highly dispersive channel - it is intended for extended range applications

The preamble is used for clock/carrier acquisition and receiver training.

1.1.2 Clause Organization

This clause is organized to follow the transmit signal path—that is, in the following order:

- *PHY Frame Format*
- *Randomization*
- *Forward Error Correction Coding and Interleaving*
- *Data modulation*
- *PHY preamble and header*
- *Baseband pulse shaping and modulation*
- *Regulatory*
- *General requirements*
- *Receiver specification*
- *UWB PHY management*

In general, this supplement does not specify the receiver but an informative clause is provided that gives some general receiver performance guidelines.

1.2 PHY Frame Format

The PHY frame format for all data rate modes is illustrated in Figure 1. The UWB PHY prepends the PHY header to the MAC header, calculates the HCS, and appends this to the MAC header. If the size of the frame body plus FCS, in bits, is not an integer multiple of the bits/symbol, then stuff bits are added following the FCS. The PHY preamble, is sent first in the packet, followed by the PHY and MAC header, followed by the MPDU and finally the tail symbols.

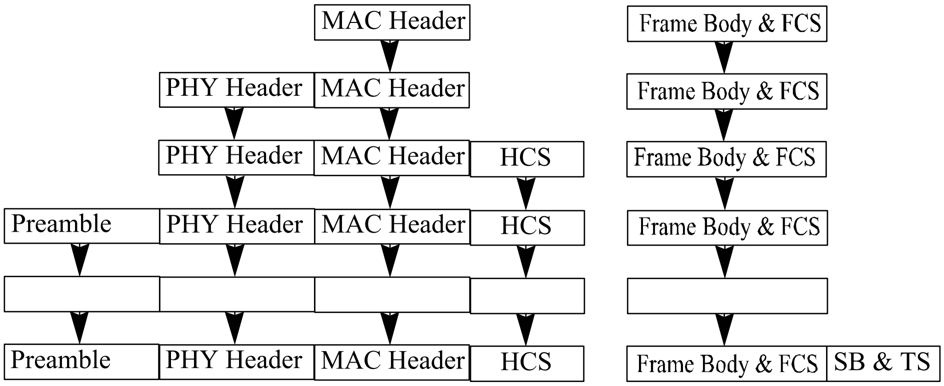

Figure 1—PHY frame formatting

1.3 Randomization

Randomization shall be employed to ensure an adequate number of bit transitions to support clock recovery. The stream of downlink packets shall be randomized by modulo-2 addition of the data with the output of the pseudo-random binary sequence (PRBS) generator, as illustrated in Figure 2.

The randomizer shall be used for the MAC header and frame body. The PHY preamble and PHY header shall not be scrambled. The polynomial, 1, for the pseudo random binary sequence (PRBS) generator shall be:

$$g(D)=1+D^{14}+D^{15} \quad (1)$$

where D is a single bit delay element. The polynomial forms not only a maximal length sequence, but also is a primitive polynomial. By the given generator polynomial, the corresponding PRBS, is generated as

$$Xn = Xn - 14 \oplus Xn - 15 \quad (2)$$

where + denotes modulo-2 addition.

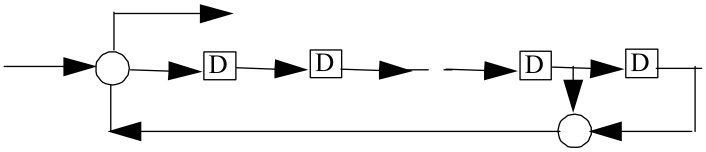

Figure 2--Realization of the randomizer linear feedback shift registers

The following sequence defines the initialization sequence,

$$x_{init}=[x^{i}_{n-1}\ x^{i}_{n-2}\ x^{i}_{n-3}\ x^{i}_{n-4}\ x^{i}_{n-5}\ x^{i}_{n-6}\ x^{i}_{n-7}\ x^{i}_{n-8}\ x^{i}_{n-9}\ x^{i}_{n-10}\ x^{i}_{n-11}\ x^{i}_{n-12}\ x^{i}_{n-13}\ x^{i}_{n-14}\ x^{i}_{n-15}] \quad (3)$$

where x^{i}_{n-k} represents the binary initial value at the output of the kth delay element.
The scrambled data bits, s_n, are obtained as follows:

$$s_n = b_n \oplus x_n \quad (4)$$

where b_n represents the unscrambled data bits. The side-stream de-scrambler at the receiver shall be initialized with the same initialization vector, x_{init}, used in the transmitter scrambler. The initialization vector is determined from the seed identifier contained in the PHY header of the received packet.

Table 1—Randomizer seed selection

Seed Identifier	Seed Value
0,0	0011 1111 1111 111
0,1	0111 1111 1111 111
1,0	1011 1111 1111 111
1,1	1111 1111 1111 111

The 15 bit seed value chosen shall correspond to the seed identifier, shown in Table 1. The seed identifier value is set to 00 when the PHY is initialized and is incremented in a 2-bit rollover counter for each packet that is sent by the PHY. The value of the seed identifier that is used for the packet is sent in the PHY header.

The 15-bit seed value is configured as follows. At the beginning of each PHY frame, the register is cleared, the seed value is loaded, and the first scrambler bit is calculated. The first bit of data of the MAC header is modulo-2 added with the first scrambler bit, followed by the rest of the bits in the MAC header and frame body.

1.4 Forward Error Correction Coding and Interleaving

The forward error correction (FEC) scheme is summarized in Table 2. A DEV shall use the DEV capabilities field to report all supported FEC rates.

Table 2—FEC code type

Code Type	**Constraint Length & Generator Polynomials**	**Possible Rates**	**Implementation Requirements**
Convolutional	Constraint length K=6, Generating polynomial (65, 57)	Rate ½ or ¾	Mandatory for Tx: Rate ½ & ¾ Mandatory for Rx: Rate ½ Optional for Rx: Rate ¾
Convolutional	Constraint length K=4, Generating polynomial (15,17)	Rate ½ or ¾	Mandatory for Tx: Rate ½ & ¾ Optional for Rx: Rate ½ & ¾

The convolutional encoder is used to encode data so that errors introduced due to noise in the channel can be corrected by the decoder. Two important characteristics of a convolutional encoder are its rate and constraint length. If k data bits are shifted in for every n encoded bits shifted out, the rate of the code equals k/n. If the maximum degree of the generator polynomials are m, then the constraint length of the code equals k(m+1). A half-rate convolutional encoder is a linear feed-forward shift register network in which, for every data bit that is shifted in, 2 encoded bits are generated. For each of the two codes specified in Table 2, the basic code is a 1/2 rate code that can be punctured to achieve a code rate of 3/4 at slightly less coding gain.

1.4.1.1 Puncturing

Higher data rates are derived from convolutional encoders by employing “puncturing.” Puncturing is a procedure for omitting some of the encoded bits in the transmitter (thus reducing the number of transmitted bits and increasing the coding rate) and inserting a dummy “zero” metric into the convolutional decoder on the receive side in place of the omitted bits. This allows a 1/2 rate code to be transformed into a 3/4 rate code. The puncturing pattern is illustrated in Figure 3. Decoding by the Viterbi algorithm is recommended.

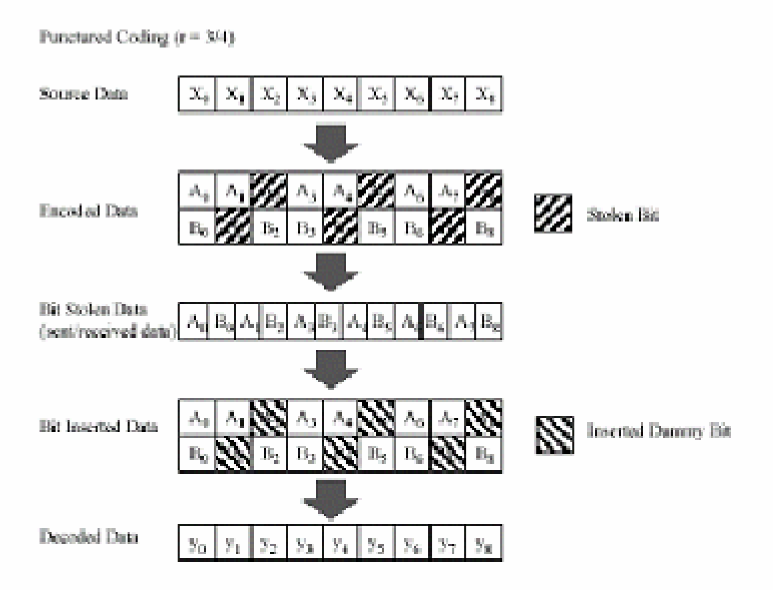

Figure 3--Puncturing

1.4.1.2 Convolutional Interleaver for Coded Bits

The convolutional decoder is sensitive to burst errors; hence, interleaving is used to disperse burst errors as shown in Figure 4:

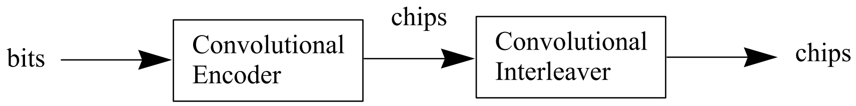

Figure 4--Convolutional Encoder with Interleaving

Convolutional interleaving is used over block interleaving because of it has lower latency and memory requirements. The structure for a convolutional interleaver is shown below in Figure 5. The encoded chips are sequentially shifted in to the bank of N registers; each successive register provides J chips more storage than did the preceding. The zeroth register provides no storage. With each new code chip the commutator switches to a new register, and the new code chip is shifted in while the oldest code chip in that register is shifted out. After the (N-1)th register, the commutator returns to the zeroth register and starts again. The deinterleaver performs the inverse operation, and the input and output commutators for both interleaving and deinterleaving must be synchronized.

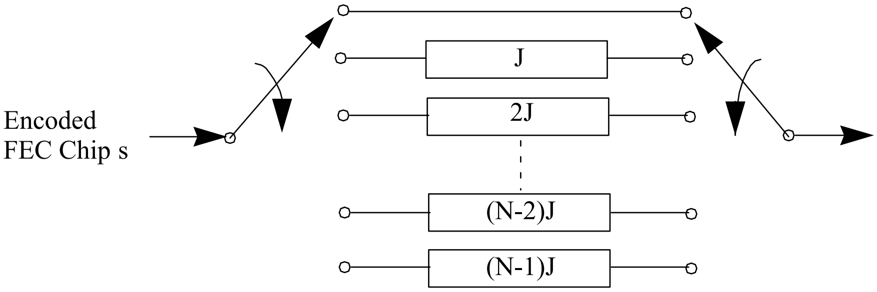

Figure 5--Convolutional Chip-wise Interleaver

The chip interleaver shall have the values of J=7 and N=10.

1.5 Data modulation

1.5.1 Data modulation using BPSK and 4-BOK

The DS-UWB proposal supports data communication using both BPSK (mandatory) and 4-BOK (optional).

BPSK modulation is low-complexity and easy to implement. Every compliant device will be able to both transmit and receive BPSK modulated signals. For some applications, it is useful to use 4-BOK to improve performance. To support these cases, every device is also required to support the *transmission* of 4-BOK modulated signals. However, it is *optional* for devices to support the capability to receive and demodulated 4-BOK modulated waveforms. This approach of requiring 4-BOK support for transmit *only* results in very low additional device complexity (generation of 4-BOK signals requires little additional complexity relative to BPSK) but it also allows implementers to incorporate the additional complexity required to receive 4-BOK signals if they desire to take advantage of the potential performance gains available in certain situations.

In the BPSK data modes, each symbol carries only a single data bit. For BPSK modulation, the data bit determines whether the spreading code with the desired length is transmitted with a polarity of either +1 or (–1).

In the 4-BOK data modes, each symbol carries two data bits. For this mode, modulation is accomplished by dividing the data bit stream into block of two bits, then mapping each block of two bits into one of two possible spreading codes for the desired data symbol rate as well as a polarity of either (+1) or (-1).

1.5.2 Available Data Rates

Table 3 and Table 4 list the data rates that are available using the lower operating band. Each data rate is achieved using the FEC rate and code length listed. Table 3 lists those modes available using BPSK modulation. Table 4 lists those modes available using 4-BOK modulation. Table 5 and Table 6 list the additional data rates that are available using the higher operating band using BPSK and 4-BOK modulation, respectively.

Data Rate	FEC Rate	Code Length	Bits per Symbol	Symbol Rate
28 Mbps	½	L=24	1	$F_{chip}/24$
55 Mbps	½	L=12	1	$F_{chip}/12$
110 Mbps	½	L=6	1	$F_{chip}/6$
220 Mbps	½	L=3	1	$F_{chip}/3$
500 Mbps	¾	L=2	1	$F_{chip}/2$
660 Mbps	1	L=2	1	$F_{chip}/2$
1000 Mbps	¾	L=1	1	F_{chip}
1320 Mbps	1	L=1	1	F_{chip}

Table 3: Available data rates using BPSK in the lower operating band.

Data Rate	FEC Rate	Code Length	Bits per Symbol	Symbol Rate
110 Mbps	½	L=12	2	$F_{chip}/12$
220 Mbps	½	L=6	2	$F_{chip}/6$
500 Mbps	¾	L=4	2	$F_{chip}/4$
660 Mbps	1	L=4	2	$F_{chip}/4$
1000 Mbps	¾	L=2	2	$F_{chip}/2$
1320 Mbps	1	L=2	2	$F_{chip}/2$

Table 4: Available data rates using 4-BOK in the lower operating band

Data Rate	FEC Rate	Code Length	Bits per Symbol	Symbol Rate
55 Mbps	½	L=24	1	$F_{chip}/24$
110 Mbps	½	L=12	1	$F_{chip}/12$
220 Mbps	½	L=6	1	$F_{chip}/6$
500 Mbps	¾	L=4	1	$F_{chip}/4$
660 Mbps	1	L=4	1	$F_{chip}/4$
1000 Mbps	¾	L=2	1	$F_{chip}/2$
1320 Mbps	1	L=2	1	$F_{chip}/2$

Table 5: Available data rates using BPSK in the higher operating band

Data Rate	FEC Rate	Code Length	Bits per Symbol	Symbol Rate
220 Mbps	½	L=12	2	$F_{chip}/12$
660 Mbps	¾	L=6	2	$F_{chip}/6$
1000 Mbps	¾	L=4	2	$F_{chip}/4$
1320 Mbps	1	L=4	2	$F_{chip}/4$

Table 6: Available data rates using 4-BOK in the lower operating band

1.5.3 Spreading codes for BPSK and 4-BOK

There are 6 piconet channels per operating band, for a total of 12 piconet channels in all. The channel numbers are listed in Table 7. A DS-UWB device is required to implement piconet channels 1-4. Support for piconet channels 5-6 in the lower band and channels 7-12 in the higher band is optional.

For each piconet channel, there is a designated chip rate (F_{chip}), a center frequency (F_{center}), and a designated set of spreading codes for use with BPSK and 4-BOK. Each piconet has 2 spreading codes for the code lengths L=24, 12, 6, 4, and 2 and only one code for the lengths of L=1 and 3. When using a BPSK data mode, each piconet uses the first spreading code listed in the table for the desired code length. When using the 4-BOK operating modes, both spreading codes of the desired length are required to modulate the data symbols.

The chip rates, center frequencies and code sets for each piconet channel are listed in Table 7. The specific spreading codes that make up each spreading code set are listed in Table 8. The relationship between the chipping rates and the carrier frequencies is always a multiple of three. The use of these offset chip rates for the different piconet channels helps to decorrelate the acquisition codes and the data symbols, in addition to facilitating piconet identification during CCA.

Piconet Channel	Chip Rate	Center Frequency	Spreading Code Set
1	1313 MHz	3939 MHz	1
2	1326 MHz	3978 MHz	2
3	1339 MHz	4017 MHz	3
4	1352 MHz	4056 MHz	4
5	1300 MHz	3900 MHz	5
6	1365 MHz	4094 MHz	6
7	2626 MHz	7878 MHz	1
8	2652 MHz	7956 MHz	2
9	2678 MHz	8034 MHz	3
10	2704 MHz	8112 MHz	4
11	2600 MHz	7800 MHz	5
12	2730 MHz	8190 MHz	6

Table 7 Piconet Channel numbers, Chip rates and Spreading code sets

Code Set Number	L=24 Codes	L=12 Codes
1	-1, 0, 1, -1, -1, -1, 1, 1, 0, 1, 1, 1, 1, -1, 1, -1, 1, 1, 1, -1, 1, -1, -1, 1	TBD
2	-1, -1, -1, -1, 1, -1, 1, -1, 1, -1, -1, 1, -1, 1, 1, -1, -1, 1, 1, 0, -1, 0, 1, 1	TBD
3	-1, 1, -1, -1, 1, -1, -1, 1, -1 , 0 -1, 0, -1, -1, 1, 1, 1, -1, 1, 1, 1, -1, -1, -1	TBD
4	0, -1, -1, -1, -1, -1, -1, 1, 1, 0, -1, 1, 1, -1, 1, -1, -1, 1, 1, -1, 1, -1, 1, -1	TBD
5	-1, 1, -1, 1, 1, -1, 1, 0, 1, 1, 1, -1, -1, 1, 1, -1, 1, 1, 1, -1, -1, -1, 0, -1	TBD
6	0, -1, -1, 0, 1, -1, -1, 1, -1, -1, 1, 1, 1, 1, -1, -1, 1, -1, 1, -1, 1, 1, 1, 1	TBD

Table 8: Length 24 and 12 spreading codes for BPSK and acquisition

Code Set Numbers	L=12 4-BOK Codes	L=6 Codes	L=4 Codes	L=3 Codes	L=2 Codes	L=1 Code
1 through 6	1,0,0,0,0,0,0,0,0,0,0,0	1,0,0,0,0,0	1,0,0,0	1,0,0	1,0	1
	0,0,0,0,0,0,1,0,0,0,0,0	0,0,0,1,0,0	0,0,1,0		0,1	

Table 9: Length 12 and shorter spreading codes for BPSK and 4BOK

1.5.4 Preamble and header modulation spreading code

The preamble PHY header and MAC header shall be modulated using the length 24 spreading code that corresponds to the appropriate piconet channel number. This length 24 spreading code for each piconet channel number is also known as the piconet acquisition code (PAC). No convolutional FEC encoder or interleaver is used for the preamble or headers.

1.6 PHY preamble and header

There are 3 preamble options that are structurally the same except for field durations:

1. A nominal preamble used for nominal data rates and channels
2. A long preamble used for low data rates and difficult channels
3. A short preamble used for high data rates and benign channels

Table 10 is used to designate the Preamble Type.

Table 10—Preamble type descriptor

Preamble Type	**b1-b0**
Medium (default)	00
Short	10
Long	11

When the Preamble Type Descriptor is used as part of an octet, the 6 upper bits are set to zero.

1.6.1 The general preamble structure

Acq Seq	TBD	Training	SFD	PHY Header	MAC Header	data
8 uS	TBD uS	4 uS	1 uS			

Figure 6--Preamble Structure

This clause presents the preamble structure, which is summarized below:

1. The TX MAC selects one of 6 piconet acquisition codes (PAC) and sets the corresponding carrier offset frequency.
2. The TX modulates the PAC code (one bit per PAC symbol) with random data to generate the acquisition sequence which is used by the receiver for initial acquisition (AGC and clock frequency lock)
3. Next is sent the training frame. The receiver uses this training frame to adjust the receiver.
4. The TX next sends the SFD (start frame delimiter) that indicates to the RX the next frame will be the PHY header, which contains rate information.
5. After the PHY header comes the MAC header.
6. Following the MAC header the TX starts sending data frames.

1.6.1.1 The piconet acquisition codeword (PAC)

There are six PAC codewords which are given in above (table 8). Each piconet uniquely uses one of these codes. The selection of the code is determined by the PNC during the initial scan prior to initiating the piconet (the PNC selects a PAC codeword that is not in use). Use of the PAC codewords provides a degree of "channel separation" between overlapping piconets during preamble acquisition, limited only by the rms cross-correlation properties of the PAC codeword set. The PAC codewords ensures that a DEV will train on the preamble associated with the "desired" piconet. Each PNC number has an associated chipping rate and carrier frequency given in Table 7.

1.6.1.2 The acquisition sequence

The preamble starts with the acquisition sequence, which is used primarily by the receiver to set gains and achieve clock synchronization. The acquisition sequence is random bits, one bit per codeword. When the acquisition sequence has been modulated by the acquistion code work, it results in a hierarchical sequence that has flat spectral properties and yet still allows relatively simple synchronization in the receier and good isolation between the different piconet channels.

1.6.1.3 The training frame

The length of the training frame varies depending upon the preamble length. Table 11 indicates the bits that shall be sent during the preamble. The bit time duration is $24/F_{chip}$ for both the low band and the high band.

The notation for Base32 is: 0123456789ABCDEFGHJKMNPQRSTVWXYZ.

Table 11—Training frame bit sequence

Preamble Type	High Band Preamble Sequence (base 32)	Low Band Preamble Sequence (base 32)
Short	TBD	TBD
Medium	JNJNB5ANB6APAPCPANASASCNJNASK9B5K6B5K5D5D5B9ANASJPJNK5MNCPATB5CSJPMTK9MSJTCTASD9ASCTATASCSANCSASJSJSB5ANB6JPAPD6B5ATASCPMNCSN5D5K6K5B9CND5JTJPBAMNK6KAMTCNJTB5N9N6N9JNMNMTJSANMSD5K9K6K9JNMNMPJSANCSN5JSK6JTJPMPJNJSASCNN5DAASB9K5MSD5B7291AT2W67PGC9Q1FNKPHH9R64FGJZRK9TYMS2KEWFCMRY31Q8NQZ8J5YNYTTS00Y87NKWHKV8J4YNPJRS2GEWQMJRSJGARPMKGHRRA84GKT1Z3J50	JNJNB5ANB6APAPCPANASASCNJNASK9B5K6B5K5D5D5B9ANASJPJNK5MNCPATB5CSJPMTK9MSJTCTASD9ASCTATASCSANCSASJSJSB5ANB6JPN5DAASB9K5MSCNDE6AT3469RKWAVXM9JFEZ8CDS0D6BAV8CCS05E9ASRWR914A1BR
Long	TBD	TBD

1.6.1.4 The start frame delimiter (SFD)

The SFD consists of the 16-bit binary pattern 0000 1100 1011 1101 (transmitted leftmost bit first) as modulation on the selected BPSK code. The first bit of the SFD follows the last bit of the sync pattern. The SFD defines the frame timing in anticipation of the PHY header.

1.6.2 PHY header

The PHY header consists of three octets that contain the number of octets in the frame body (including the FCS), the data rate of the frame body and seed identifier for the data scrambler. The fields for the PHY service field are shown in Table 12. Bit b0 is sent over the air first and the other bits follow sequentially.

Table 12—PHY service field

Bits	Content	Description
b0-b1	Seed Identifier	2 bit field that selects the seed for the data scrambler, defined in Table X
b2-b4	FEC Type	3 bit field that indicates the FEC type 000 = no FEC 001 = k=6, rate 1/2 Convolutional code 010 = k=6, rate 3/4 Convolutional code 011 = k=4, rate 1/2 Convolutional code 100 = k=4, rate 3/4 Convolutional code 101 = Reserved for future use 110 = Reserved for future use 111 = Reserved for future use
b5	Interleaver Type	1 bit field that indicates the interleaver type 0 = Convolutional bit interleaver 1 = Reserved for future use
b6-b8	Payload code length	3 bit field that indicates the spreading code length 000 = Code length 24 001 = Code length 12 010 = Code length 6 011 = Code length 4 100 = Code length 3 101 = Code length 2 110 = Code length 1 111 = Reserved for future use
b9	Modulation type	1 bit field that indicates the modulation type 0 = BPSK 1 = 4-BOK
b10-b23	Frame Body Length	A 14 bit field that contains the length of the frame body, in octets, MSB is b5, LSB is b15, e.g. 4 octets of data, is encoded as 0b00000000100. A zero length frame body is encoded as 0b000000000000 and there is no FCS for this packet.

1.6.3 MAC header

The MAC header is unchanged from the IEEE Std 802.15.3™-2003.

1.6.4 Header check sequence

The header check sequence is calculated on the combined PHY and MAC Headers. The header check sequence is appended after the MAC header and contains the 16 bit CRC for the combined PHY and MAC headers. The polynomial used is:

$$x^{16} + x^{12} + x^{5} + 1 \quad (5)$$

This CRC is the same one used in IEEE Std 802.11b-1999.

1.6.5 Preamble length considerations

1.6.5.1 Preamble field lengths

Table 13 defines the preamble field lengths for each of the preamble duration options.

Table 13—Preamble field octets

	Nominal Preamble	**Long Preamble**	**Short Preamble**
Acquisition Sequence	445	1780	445
Sync Burst	12	12	12
Training Sequence	445	1780	220
SFD	2	2	2
PHY Header	2	2	2
MAC Header	TBD	TBD	TBD
HCS	TBD	TBD	TBD

1.6.5.2 Field data rates

All fields of the preamble are sent at the base rate.

1.7 Baseband pulse shaping and modulation

1.7.1 Baseband impulse response

The baseband reference pulse is a root raised cosine low pass filter with 30% excess bandwidth. For both the low and high frequency bands the filter cutoff frequency (-3 dB point) is $F_{chip}/2$.

The implemented baseband impulse response must have a peak cross-correlation within 3 dB of the reference pulse.

1.7.2 Reference spectral mask

The reference spectral mask is shown in Figure 7. Out-of-band emissions must meet the regulatory dom

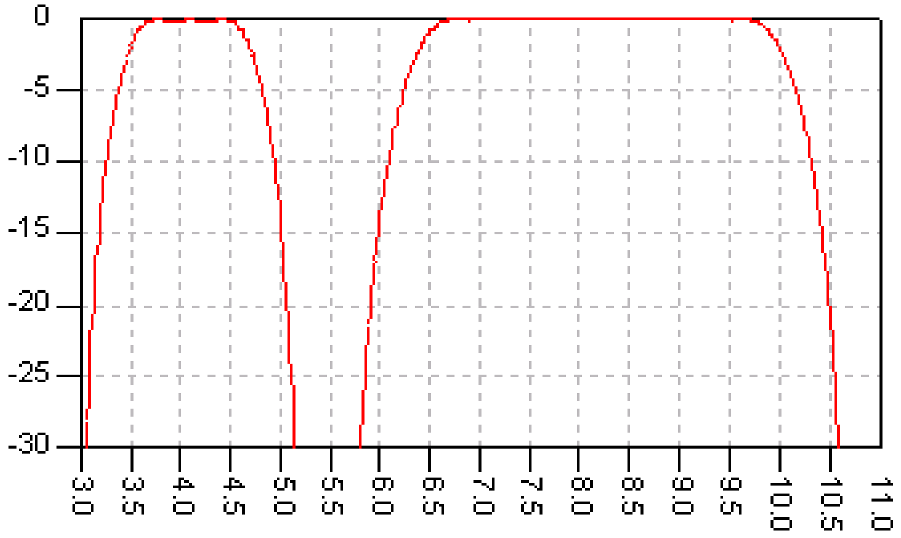

Figure 7--Super-impose Lower and Upper Band Reference Pulse Spectral Mask

1.7.3 Chip rate clock and chip carrier alignment

The chip rate clock and the chip carrier shall be provided from the same source. The accuracy required is 25 ppm.

1.8 Regulatory

1.8.1 Regulatory compliance

The maximum allowable output power spectral density, as measured in accordance with practices specified by the appropriate regulatory bodies, is shown in Table 14.

Table 14—Maximum transmit power levels

Geographical Region	Power Limit	Regulatory Document
Japan	TBD	ARIB STD-xxx
Europe (except Spain and France)	TBD	ETS xxx
USA	-41.3 dBm/MHz	47 CFR 15.xxx

1.9 General requirements

1.9.1 Channel assignments

A total of 12 logical channels are assigned for operation, 6 channels per band with two bands. A compliant IEEE Std 802.15.3™-2003 implementation shall support at least channel numbers 1-4 in the low band of operation and optionally bands 5-6 in the low band and/or bands 7-12 in the high band. The piconet channel numbers are shown in Table 7 along with the associated carrier frequencies and chip rates.

1.9.2 Operating temperature range

A conformant implementation shall meet all of the specifications in this standard for ambient temperatures from 0 to 40 C.

1.9.3 Interframe spacing

A conformant implementation shall support the interframe spacing parameters given in Table 15.

Table 15—Interframe spacing parameters

802.15.3 MAC Parameter	Corresponding PHY parameter	Definition
SIFS	aRXTXTurnaroundTime	TBD

1.9.4 Receive-to-transmit turnaround time

The RX-to-TX turnaround time, aRXTXTurnaroundTime, shall be no less than TBD µs and no more than TBD µs. The RX-to-TX turnaround time shall be measured at the air interface from the trailing edge of the last symbol received until the first symbol of the PHY preamble is present at the air interface.

1.9.5 Transmit-to-receive turnaround time

The TX-to-RX turnaround time shall be less than TBD µs. The TX-to-RX turnaround time shall be measured at the air interface from the trailing edge of the last transmitted symbol until the receiver is ready to begin the reception of the next PHY packet.

1.9.6 Maximum frame length

The maximum frame length allowed, pMaxFrameSize, shall be 4096 octets. This total includes the frame body and FCS but not the PHY preamble, PHY header or MAC header.

1.9.7 Transmit power control

A compliant transmitter is allocated power on a power density basis. It shall be capable of transmitting no more than -2.5 dBm (TBR) and shall be capable of reducing its power to less than -10 dBm in monotonic steps no smaller than 3 dB and no larger than 5 dB. The steps shall form a monotonically decreasing sequence of transmit power levels. A compliant device shall have its supported power levels indicated in its PHY PIB based on its maximum transmit power and power level step size.

The minimum TX power level required to support TPC, aMinTPCLevel, shall be -10 dBm.

1.9.8 Transmit center frequency tolerance

The transmitted center frequency tolerance shall be ±25 ppm maximum.

1.9.9 Symbol clock frequency tolerance

The symbol clock frequency tolerance shall be ±25 ppm maximum.

1.9.10 Clock synchronization

The transmit center frequency and the symbol clock frequency shall be derived from the same reference oscillator.

1.10 Receiver specification

1.10.1 Error rate criterion

The error rate criterion shall be a packet error ratio (PER) of less than 8% with an frame body length of 1024 octets of pseudo-random data generated with a PN23 sequence as defined in $x_{n+1} = x_n^{23} + x_n^{5} + 1$. Note that the packets used for measuring the error rate criterion include not only the frame body of 1024 octets, but also the PHY preamble, PHY header, MAC header and the FCS.

1.10.2 Receiver sensitivity Receiver sensitivity

For a packet error rate (PER) of less than 8% with a PSDU of 1024 bytes, the minimum receiver sensitivity numbers for the various rates and modes are listed in Table 16.

Table 16 – Receiver performance requirements

Data rate (Mbps)	Minimum sensitivity (dBm)
28	-85.5
55	-82.5
110	-79.5
220	-76.5
500	-71.4
1000	-68.4

1.10.3 Receiver CCA performance

The start of a valid OFDM transmission at a receiver level equal to or greater than the minimum 110 Mbps sensitivity shall cause CCA to indicate busy with a probability > 90% within 5 microseconds. If the preamble portion was missed, the receiver shall hold the carrier sense (CS) signal busy for any signal 20 dB above the minimum 110 Mbps sensitivity.

1.10.4 Receiver maximum input level

The receiver maximum input level is the maximum power level of the incoming signal, in dBm, present at the input of the receiver for which the error rate criterion is met. A compliant receiver shall have a receiver maximum input level of at least -20 dBm for each of the modulation formats that the device supports.

1.10.5 Receiver RSSI

RSSI is defined as the power relative to the maximum receiver input power level, in 8 steps of 8 dB with +/- 4 dB step size accuracy. The range covered shall be a minimum of 40 dB. The steps shall be monotonic. The RSSI power shall be the average power measured during the training sequence of the PHY preamble. This number shall be reported via the PHY-RXSTART.indication.

1.11 UWB PHY management

The PHY PIB comprises the managed objects, attributes and notifications required to manage the PHY layer of a DEV.

The PHY dependent PIB values for the UWB PHY are given in Table 17.

Table 17—UWB PHY PIB parameter definitions

PIB Parameter	Value
PHYPIB_RSSI_max	TBD
PHYPIB_LQI_max	TBD
PHYPIB_NumTxPowerLevels	TBD
PHYPIB_PowerLevelVector	TBD
PHYPIB_CCA_Threshold	TBD

There are 3 fields related to supported PHY data rates in the Capability IE: the Supported RX Data Rates field, the Supported TX Data Rates field, and the Bands Supported field. The RX and TX supported rates fields are described in Table 18.

Table 18—UWB PHY supported data modes

Bits	Content	Description

b0-b1	FEC Type	2 bit field that indicates supported FEC types 00 = no FEC 01 = Convolutional FEC with k=6 10 = Convolutional FEC with k=4 11 = reserved for Future Use
b2-b3	Spreading Codes	2 bit field that indicates supported code word lengths 00 = Code word lengths 6, 12 and 24 01 = Code word lengths 3, 4, 12, and 24 10 = Code word lengths 2, 3, 4, 12 and 24 11 = Code word lengths 1, 2, 3, 4, 12 and 24
b4	Modulation	1 bit field that indicates supported modulation types 0 = BPSK only for receive 1 = BPSK and 4-BOK for receive

The Bands Supported field is described in Table 19.

Table 19—Bands supported

Supported Bands	**b0**
Only Low Band	0
Both Low and High Bands	1