Project: IEEE P802.15 Study Group for Wireless Personal Area Networks (WPANs)

Submission Title:  PSSS proposal – Parallel reuse of 2.4 GHz PHY for the sub-1 GHz bands
Date Submitted:  17 November 2004
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Re:  Analysis of PSSS for higher data rates for PHY for sub-1 GHz

Abstract:  The proposed parallel reuse of the 2.4 GHz 802.15.4 modulation technology in PSSS offers highly attractive performance improvement, fulfills all key OEM requirements, and visibly increases market opportunities.

Purpose:  Further analysis of PSSS as in accepted joint PHY proposal from September 2004

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PSSS Proposal

Parallel reuse of 2.4 GHz PHY for the sub-1-GHz bands

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STS
Presentation Contents

• Introduction
  – Summary of OEM requirements for the TG4b PHY

• PSSS variants reviewed in this document

• PSSS Performance
  – BPSK / ASK modulation
  – O-QPSK / I/Q modulation

• PSSS Implementation aspects
  – Crystal quality – frequency offset tolerance
  – PSD
  – Chip size and power consumption

• Status

• Summary

• Attachments
  – PSSS PHY Tx operation
  – Selected Rx implementation options
  – Linearity
Key requirements for sub-1-GHz band PHY

- **Bitrate over 200 kBit/s**
  - Number of permitted transactions/hr is insufficient in IEEE802.15.4-2003 868 Mhz
  - 1% duty cycle at 20 kbit/s translates into typically only 600-800 transactions/hr
  - With > 200 kbit/s sufficient number of transactions/hr for our targeted applications
  - Disadvantage of 1% duty cycle limit turns into *protection against interference*
  - Extension from 20/40 kbit/s extends total battery lifetime by 15-40%

- **Visibly improved multipath fading robustness over IEEE802.15.4-2003 2.4 GHz**
  - Improve coverage in “challenging” RF environments – Especially commercial, industrial
  - Achieve PER < 10⁻³ at channels with at least 1 µs delay spread (non-exponential channel models)

- **Support of current RF regulatory regimes plus enable the use of extended bands**
  - Support 2 MHz wide channels in the USA and other countries were they are permitted
  - Support of current 600 kHz band available at 1% duty cycle in Europe today
  - Allow use of extended European bands and bands in other countries once they become available
    - Allow addition of additional 600 kHz channels as per current ETSI / ECC report (4/6 channels?)
    - Do not expect US-like wide, unrestricted bands or all egulatory domains
  - Support of more flexible channel selection method to flexibly add support for more countries

- **Backward compatibility to IEEE802.15.4-2003 (915/868 MHz)**
  - Interoperability when switched to 15.4-2003 mode
  - No fully transparent backward compatibility as in 802.11b vs. 802.11 or 802.11g vs. 802.11b

- **Low cost and low power consumption (!)**
# PSSS variants reviewed in this presentation

<table>
<thead>
<tr>
<th></th>
<th>PSSS 234-600</th>
<th>PSSS 225-600</th>
<th>PSSS 210-600</th>
<th>PSSS 250-600 a/b</th>
<th>PSSS 250-2000</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bandwidth</strong></td>
<td>600 kHz</td>
<td>600 kHz</td>
<td>600 kHz</td>
<td>600 kHz</td>
<td>2,000 kHz</td>
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<tr>
<td><strong>Chiprate</strong></td>
<td>500 cps</td>
<td>480 cps</td>
<td>450 cps</td>
<td>266.6 / 400 cps</td>
<td>800 kcps</td>
</tr>
<tr>
<td><strong>Bitrate</strong></td>
<td>234 kit/s</td>
<td>225 kbit/s</td>
<td>210 kbit/s</td>
<td>250 kbit/s</td>
<td>250 kbit/s</td>
</tr>
<tr>
<td><strong>Spectral efficiency</strong></td>
<td>15/32 bit/s/Hz</td>
<td>15/32 bit/s/Hz</td>
<td>15/32 bit/s/Hz</td>
<td>0.9375 / 0.625 bit/s/Hz (30/32; 20/32)</td>
<td>0.3125 bit/s/Hz (10/32)</td>
</tr>
<tr>
<td><strong>Spreading</strong></td>
<td>15x 32-chip seq.</td>
<td>15x 32-chip seq.</td>
<td>15x 32-chip seq.</td>
<td>10x 32/15x32-complex chip seq.</td>
<td>5 x 32 complex chip seq.</td>
</tr>
<tr>
<td><strong>RF backward compatibility</strong></td>
<td>Single BPSK / ASK radio</td>
<td>Single BPSK / ASK radio</td>
<td>Single BPSK / ASK radio</td>
<td>IQ radio</td>
<td>IQ radio</td>
</tr>
<tr>
<td><strong>Comments</strong></td>
<td>Original mode in joint proposal</td>
<td>Added upon TG4b request to have “more even” bitrate</td>
<td>Added upon chip manufacturer input to reduce complexity / costs</td>
<td>Added as variant based on I/Q modulator + low cost 250 kbit/s in 600 KHz</td>
<td>Added as variant to show that use of PSSS is also attractive in 2 MHz channels</td>
</tr>
</tbody>
</table>

**Note:**
DWA fully supports the accepted joint proposal - variants are provided to provide a more comprehensive analysis.

Choice to be discussed in TG4b
Challenges in comparison of PHY variants in TG4b PHY subcommittee

- Uneven level of analysis and scrutiny between PSSS and COBI
  - Despite major deviation from IEEE802.15.4-2003 2.4 Ghz design, many implementation challenges are not yet reviewed for COBI, e.g. synchronization, PSD, required linearity, Rake receiver

- Current COBI simulations discussed are not suitable to drive conclusions
  - Limited, incomplete simulation model – e.g. without preamble, synchronization
  - Critical parts of Rake receiver are not simulated (furthermore, experience is that even full Rake simulations deviate significantly from actual implementations – commonly accepted in scientific literature)
  - Switch from agreed comparison of PER to BER (focus on irrelevant BER values)
  - COBI8 variants shown cannot fulfill ETSI spectrum mask (Nyquist)

- Unclear PSSS simulations from IIR
  - Results from September 2004 and now are inconsistent
  - PSSS without precoding is shown with lower performance than with precoding
  - PSSS is shown with unnecessary Rake receivers driving irrelevant and misleading conclusions
Simulation models used

**Simulation model used by DWA**

- PN Data
- Preamble + FD Generation
- PSSS Encoder + Precoding
- Pulse Shaping
- Modulator
- MP + AWGN Channel
- Demodulator
- AGC
- PSSS Decoder
- PER Measurement
- Chip Synchronization

**Simulation model used by IIR in TG4b PHY discussions**

- PN Data
- Preamble + FD Generation
- COBI / PSSS Encoder
- Pulse Shaping
- Modulator
- MP + AWGN Channel
- Demodulator
- AGC
- COBI / PSSS Decoder
- PER Measurement
- Chip Synchronization
- Rake Channel Estimation etc.

- Agreed simulation model used by DWA:
  - **Discrete exponential model**
    - Sampled version of diffuse model (high sampling rate)
    - At least 1000 random channel realizations
    - **PER** calculated on complete PPDUs with preamble and FD
- **Notes:**
  - Results shown by IIR for COBI8 are based on model with PSD that violates ETSI
  - **BER** of only 10^{-3} / 10^{-4} shown is insufficient for target market – **PER** of 10^{-3} is typically used in IEEE802
  - COBI Rake receiver structure unclear
  - Preamble proposed by IIR for COBI16/8 is inappropriate for use with rake (i.e. too short for accurate channel estimation)
  - Is preamble proposed sufficient for other COBI modes?
  - **Rake receiver requires higher accuracy for AGC and linearity. Effects have to be investigated.**
Earlier results of basic model also used by IIR

Source: Halfrate 2.4 GHz: IEEE 15-04-337-00-004b, Motorola, slide 6

Channel with 0ns RMS delay spread differs from “no fading” due to channel model characteristic
Channel Response – Simulation of 1429 Frames used by DWA

Real Part

Imaginary Part

Note:
Actual channels in industrial and commercial environments are having significantly higher probability for non-exponential amplitude/time than assumed in the agreed and used model
PSSS – BPSK/ASK variant\(^1\) (15/32 bit/s/Hz) simulated

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**Diagram:**

- **Bit-to-Symbol Mapper**
- **Symbol-to-Chip Mapper**
- **Combiner**

**Input Data:**

- 15
- 0 / 1 bits
- \(-1 / 1\)

**Base sequence:**

- Selected 15 shifted sequences

**Addition:**

- Addition of per-row multiplication result plus precoding

**Sequence with 32 chips per Symbol**

---

1: PSSS 225-600 + PSSS 210-600
2: Use of single base sequence simplifies implementation in Rx
PER Performance PSSS BPSK/ASK variant – Discrete Exponential Channel, 370ns RMS Delay Spread

- Over 12 dB performance benefit in relevant PER range
  - Even higher benefit in environments with higher MP fading challenges
- COBI16 performance is estimated to be 4...7dB weaker than even COBI16
  - Little if any performance benefit over 868MHz FSK chips

PSSS fulfills performance requirements without adding complexity, cost, and power consumption for rake receivers

- PSSS 225 kbit/s  — COBI16+1 235 kbit/s  > 10000 Channel, no Rake receivers
PSSS – 250 kbit/s I/Q variant 1 (IQ1) simulated

Bit-to-Symbol Mapper
Symbol-to-Chip Mapper
Combiner

Input Data

2x 15
0 / 1 bits
-1 / 1

Base sequence
Selected 15 shifted complex sequences

32

15 sequences

32

Pulse shaping

I/Q modulator

Sequence with 32 complex chips per Symbol

... simplest pulse shaping enabling very low cost implementation

1: PSSS 250-600a
PSSS – 250 kbit/s I/Q variant 2 (IQ2) simulated

... enables reuse of chip designs with I/Q modulator / demodulator

1: PSSS 250-600b
PER Performance PSSS IQ variants – Discrete Exponential Channel, 370ns RMS Delay Spread

Similar and even higher benefit over COBI16

- PSSS 225 kbit/s
- COBI16+1 coherent, 235 kbit/s
- PSSS IQ1 (250-600a)
- PSSS IQ2 (250-600b)
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Crystal quality – Tolerated frequency offset

- Performance against frequency offset –
  *Original target in TG4: Up to ±40ppm*

  - Assumptions for chip clock:
    - PDU length 127 Byte = 8*127 bit = 1016 bit
    - 15 bit per PSSS Symbol (32 chip)
    - \( \rightarrow 68 \) PSSS Symbols with 2176 chips (Chip duration \( T_c = 2\mu s \))

  - Results
    - 40ppm for 2176 chips = \( 0.087 \) chip error for the whole PDU
    - For one PSSS Symbol with 32 chips
      the error is about 40ppm*32 chip = \( 0.00128 \) chip

⇒ No influence to PSSS Performance by ±40ppm and worse crystal
Crystal quality – Tolerated frequency offset – Measurements from PSSS prototype

0.1% Chip Clock Error

1% Chip Clock Error

Yellow: 0% chip clock error reference signal
Pink: 0.1% and 1% chip clock error

Calculation of crystal quality tolerance confirmed with prototype
Simulation models used for pulse shaping

**Passband pulse shaping model**

- PSSS Encoder → Non Linearity → Pulse Shaping → PSD

**Baseband pulse shaping model**

- PSSS Encoder → Pulse Shaping → Non Linearity → PSD

**Notes:**
- Pulse shaping per draft specification text provided submitted by DWA
- Details of models conformant to ETSI recommendations
- Actual bandwidth for PSD 16 kHz simulation
- Square root raised cosine filter $r=0.1$
  - Theoretical limit $r=0.2$
  - ETSI power limits are absolute $+14$ dBm inband, $-36$ dBm outband
    - For simulation assumed to send with max. power $+14$ dBm
    - Therefore simulation results contain relative PSD levels
      - $+14$ dBm $\rightarrow$ 0 dB
      - $-36$ dBm $\rightarrow$ -50 dB
Non Linear Transfer Function –
Passband pulse shaping

Used transfer function for simulating PSD for non linearity
Non Linear Transfer Function – Baseband pulse shaping

Used transfer function for simulating PSD for non linearity
PSD PSSS Signal –
Passband pulse shaping, linear, no precoding

Simulations of the relative PSD in dB for the PSSS signal at 450 kchips/s, 210 kbit/s, +/- 40ppm.
PSD PSSS Signal –
Passband pulse shaping, linear, precoding

Simulations of the relative PSD in dB for the PSSS signal at 450 kchips/s, 210 kbit/s, +/- 40ppm.

Conform to ETSI limits
PSD PSSS Signal –
Passband pulse shaping, non linear, no precoding

Simulations of the relative PSD in dB for the PSSS signal at 450 kchips/s, 210 kbit/s, +/- 40ppm.

Conform to ETSI limits
PSD PSSS Signal – Passband pulse shaping, non linear, precoding

Simulations of the relative PSD in dB for the PSSS signal at 450 kchips/s, 210 kbit/s, +/- 40ppm.
PSD PSSS Signal –
Passband pulse shaping, linear, no precoding

Simulations of the relative PSD in dB for the PSSS signal at 480 kchips/s, 225 kbit/s, +/- 20ppm. Conditions: linear, no precoding

Conform to ETSI limits
PSD PSSS Signal – Passband pulse shaping, linear, precoding

Simulations of the relative PSD in dB for the PSSS signal at 480 kchips/s, 225 kbit/s, +/- 20ppm. Conditions: linear, precoding

Conform to ETSI limits
PSD PSSS Signal –
Passband pulse shaping, non linear, no precoding

Simulation of the relative PSD in dB for the PSSS signal at 480 kchips/s, 225 kbit/s, +/- 20ppm.

Conditions: non linear, no precoding
PSD PSSS Signal –
Passband pulse shaping, non linear, precoding

Simulations of the relative PSD in dB for the PSSS signal at 480 kchips/s, 225 kbit/s, +/- 20ppm.
Conditions: non linear, precoding

Conform to ETSI limits
PSD PSSS Signal –
Baseband pulse shaping, non linear, precoding

Simulations of the relative PSD in dB for the PSSS signal at 450 kchip/s 210 kbit/s, +/- 40ppm

Conform to ETSI limits
PSD PSSS Signal –
Baseband pulse shaping, non linear, precoding

Simulations of the relative PSD in dB for the PSSS signal at 480 kchip/s, 225 kbit/s, +/-20 ppm

Conform to ETSI limits
# PSSS IQ1 Mode

<table>
<thead>
<tr>
<th>#</th>
<th>Code</th>
<th>Spectral Efficiency</th>
<th>Data Rate kbs</th>
<th>Chiprate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0.625</td>
<td>250</td>
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<tr>
<td>10</td>
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</table>

Simulations of the relative PSD in dB for the PSSS signal at 400 kchip/s 250 kbit/s.
Conditions: linear, precoding, +/-40 ppm, r = 0.25 roll on off

Conform to ETSI limits
PSSS IQ 2 Mode

<table>
<thead>
<tr>
<th>#</th>
<th>Code #</th>
<th>Spectral Efficiency</th>
<th>Data Rate kbs</th>
<th>Chiprate</th>
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<tbody>
<tr>
<td>1</td>
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</table>

Simulations of the relative PSD in dB for the PSSS signal at 266 kchip/s 250 kbit/s.
Conditions: linear, precoding, +/-40 ppm, r = 1 roll on off

Conform to ETSI limits
Simulations of the relative PSD in dB for the Cobi at 500 kchip/s, 250 kbit/s, r = 0.2, +/-40 ppm.

Reference for COBI 8: IEEE 802.15-04-0586-05-004b , slide 5
PSD for COBI8 in 600 KHz channel
Baseband pulse shaping non-linear

Simulations of the relative PSD in dB for the Cobi at 500 kchip/s, 250 kbit/s, r = 0.2, +/-40 ppm.

Reference for COBI 8: IEEE 802.15-04-0586-05-004b, slide 5
PSD for COBI8 in 600 KHz channel
Baseband pulse shaping linear

Simulations of the relative PSD in dB for the Cobi at 400 kchip/s, 200 kbit/s, r = 0.5, +/-40 ppm.

Reference for COBI 8: IEEE 802.15-04-0586-05-004b, slide 5
PSD for COBI8 in 600 KHz channel
Baseband pulse shaping non-linear

Simulations of the relative PSD in dB for the Cobi at 400 kchip/s, 200 kbit/s, r = 0.5, +/-40 ppm.

Reference for COBI 8: IEEE 802.15-04-0586-05-004b, slide 5
Simulations of the relative PSD in dB for the Cobi at 300 kchip/s, 150 kbit/s, $r = 1$, +/-40 ppm.

Reference for COBI 8: IEEE 802.15-04-0586-05-004b, slide 5
PSD for COBI8 in 600 KHz channel
Baseband pulse shaping non-linear

Simulations of the relative PSD in dB for the Cobi at 300 kchip/s, 150 kbit/s, \( r = 1 \pm 40 \text{ ppm} \).

Reference for COBI 8: IEEE 802.15-04-0586-05-004b, slide 5
Crystal quality, Linearity, PSD – Conclusions

• **Crystal Quality conclusions**
  – PSSS could work in ETSI mask with +/-40ppm tolerance up to 250 kbit/s, depending of used coding

• **PSD Conclusions**
  – PSSS matches with with up to 450/480 kchip/s (40/20 ppm) the ETSI recommendations
  – Depending on pulse shaping passband / baseband Non-Linearity 20% / 1%
    has nearly no effect to PSD
  – PSD for COBI81 at 250 kbit/s violates ETSI recommendations
  – Non linearity increases also outband PSD for COBI

• **General Linearity Conclusions**
  – PSSS works even with 20% non linear PA and LNA
  – PA designs are available off-the-shelf with
    • No increase in chip cost even for linearity of 2%
    • No additional power consumption compared to C class PA used in IEEE802.15.4-2003 today
  – No impact of linearity requirements on power consumption
    • Reviewed and confirmed with two large semiconductor manufacturers
  – No implementation risk due to increased linearity required for PSSS !

• **Non-linearity simulations are confirmed with PSSS prototype**
  1) Reference: IEEE 802.15-04-0586-05-004b, slide 5
## Chip size and power consumption

### Chip size

- High tolerance towards non-linearity and simplicity of PSSS minimizes increase in analog part
  - Estimate 0.25 mm² max.
- Digital part: No increase expected due to reduced complexity.

**Total increase:** 7-10 % PHY max.
4-6 % TRx die
2-3 % SoC die
< 2% SoC cost!

- Larger increase in size expected for COBI for Rake receiver etc.

### Power consumption

- High tolerance against non-linearity and simplicity of PSSS minimizes increase in power consumption
  - Estimate Rx/Tx: 5-10% max.
  - Sleep: <0.05 µA
- 15.4 2.4 Ghz chips today spread between 15...55 mA Rx
  - Effect of implementation + process is large vs. increase from PSSS (if any)

**No visible change in battery lifetime**
- Most energy for sleep+discharge
- Longer battery life vs. current 868/915

- Visible increase expected for COBI due to Rake receiver etc.

Assumption: 0.18 µ CMOS process
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Status

• Comprehensive research and development on PSSS has been performed based on:
  – Full simulation
  – Configurable prototype for PSSS
  – Analytical model for PSSS

Minimal risk for implementation due to well understood technology and all building blocks being widely available
Results of first field measurements with PSSS and COBI16:
Residential / light commercial environments –
Small office building, heating application

• Test site: Office building (brick, sheetrock walls), rms delay spreads typ. 200 ... 400 ns
• Tested RF technology:
  – IEEE802.15.4-2003 (2.4 GHz), 0dBm Tx
  – PSSS 225-600, 225 kbit/s (600 kHz) in 2.4 Ghz, 0dBm Tx
  – COBI16+1, 235 kbit/s (600 kHz) in 2.4 GHz, 0 dBm Tx
<table>
<thead>
<tr>
<th></th>
<th>PSSS 225-600</th>
<th>PSSS 210-600</th>
<th>PSSS 250-600 a/b</th>
<th>PSSS(^1) 250-2000</th>
<th>COBI16(^2)</th>
<th>COBI8(^2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>600 kHz</td>
<td>600 kHz</td>
<td>600 kHz</td>
<td>2,000 kHz</td>
<td>2,000 kHz</td>
<td>600 kHz</td>
</tr>
<tr>
<td>Chiprate</td>
<td>480 cps</td>
<td>450 cps</td>
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<td>Bitrate</td>
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<td>250 kbit/s</td>
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<tr>
<td>Spreading</td>
<td>15x 32-chip seq.</td>
<td>15x 32-chip seq.</td>
<td>10/15x 32-chip seq.</td>
<td>5x 32 chip seq.</td>
<td>16x16 chip seq.</td>
<td>16x8 chip seq.</td>
</tr>
<tr>
<td>Pulse shape</td>
<td>Square root raised cosine (r = 0.2)</td>
<td>Square root raised cosine (r = 0.2)</td>
<td>Square root raised cosine (r = 0.5 / 0.2)</td>
<td>Square root raised cosine (r = ?)</td>
<td>Halvsine</td>
<td>Raised cosine (R = 0.2) Not possible(^3)</td>
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<tr>
<td>Rake</td>
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<td>Not required</td>
<td>Not required</td>
<td>Not required</td>
<td>Required(^1)</td>
<td>Required(^1)</td>
</tr>
<tr>
<td>Modulation</td>
<td>BPSK + ASK</td>
<td>BPSK + ASK</td>
<td>BPSK + I/Q</td>
<td>BPSK + ASK</td>
<td>OQPSK</td>
<td>BPSK</td>
</tr>
<tr>
<td>Complexity</td>
<td>small</td>
<td>small</td>
<td>Small to medium</td>
<td>small</td>
<td>high</td>
<td>high</td>
</tr>
<tr>
<td>MP performance (E_b/N_0 @ \text{PER}=10^{-3})</td>
<td>31dB</td>
<td>31dB</td>
<td>27dB/30dB</td>
<td>?</td>
<td>&gt;&gt;40dB</td>
<td>&gt;&gt;&gt;40dB</td>
</tr>
<tr>
<td>Conclusion</td>
<td>Attractive</td>
<td>Highly Attractive</td>
<td>Attractive</td>
<td>Highly Attractive</td>
<td>Less Attractive</td>
<td>Not Attractive</td>
</tr>
</tbody>
</table>

1): Not yet fully simulated, may still not provide required MP performance
3): Also other proposed COBI8 versions are not conform to ETSI rec.
Summary

• PSSS is the only proposal that fulfills all OEM requirements
  – Provides very high robustness against MP fading – up to 2 µs
    i.e. visibly stronger MP fading robustness than current 2.4 GHz PHY,
    provides required higher range in many attractive, high volume target areas
  – Data rate of > 200 kbit/s at low complexity with highly backward compatible PHY,
    250 kbit/s with even simpler pulse shaping with I/Q modulation/demodulation
  – Suitable for existing and upcoming regulatory environment in Europe (ETSI)

• Analysis in TG4b has shown that PSSS is implementable at low risk
  – High confidence in results due to very comprehensive simulation model
  – Simulation results match first measurements with lab prototype
  – Full understanding of PSD shows compliance with stringent ETSI requirements

• PSSS offers highly attractive performance and increases market opportunities
  – Performance of COBI is lower than with current 2.4 GHz PHY coding
  – PSSS is competitive with Bluetooth radios in industrial / commercial environments

• PSSS provides for Europe significantly more attractive solution than COBI
  – Lower COBI16 performance is acceptable for US
    *if* higher permitted Tx power is used (only if feasible with regard to PSD!)
  – Use of Rake receiver is inconsistent with IEEE802.15.4 objectives
Attachments
Changes vs. PSSS presentation
at March 2004 meeting (Orlando)

- **Unchanged basic proposal for parallel reuse of 2.4 GHz PHY!**
  - Added option of use of BPSK/ASK instead of O-QPSK
    - Based on OEM and semiconductor manufacturers requirements
    - To avoid added complexity and cost for two radio cores
    - To avoid doubling required bandwidth for O-QPSK
  - Added option to reduce 868 Mhz bandwidth to 500 Khz
    - Changed to reduce implementation complexity and cost
    - Bitrate of 234 kbit/s changed to 225 kbit/s based on input from September 2004 meeting to have “more even” bit rate
    - 210 kbit/s and 250 kbit/s variants added based on chip manufacturer’s inputs in TG4b PHY subcommittee to even further reduce implementation cost
  - Details of combining provided that were not shown in March 2004
    - Coding gain through simple precoding in combiner

- **Added new results on PSSS**
  - Solution performance
  - Implementation aspects
  - Status
Used Matlab Code for Discrete Channel

L=2
% L=2 equal 370 ns RMS Delay Spread
profile = zeros(1,10*L+1);
profile(1:L:end) = exp(-(0:10)/2);
profile = profile/(sum(profile));
channel = sqrt(profile/2).*(randn(size(profile))+j*randn(size(profile)));
signal_out = zeros(size(signal_in));
for k = 0:10
    signal_out=signal_out+channel(k+1)*[zeros(1,k*L) signal_in(1:length(signal_in)-k*L)];
end

Source:
Paul Gorday Freescale IEEE 802.15-04-0585-00-004b, slide 9
PSSS –
Tx – BPSK/ASK variant (15/32 bit/s/Hz)$^1$

---

$^1$: PSSS 225-600 + PSSS 210-600

2: Use of single base sequence simplifies implementation in Rx
## Symbol-to-Chip Mapper

<table>
<thead>
<tr>
<th># Bit</th>
<th>Chip Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>-1 -1 -1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
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</tr>
<tr>
<td>3</td>
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</tr>
<tr>
<td>4</td>
<td>1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
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</tr>
<tr>
<td>6</td>
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</tr>
<tr>
<td>7</td>
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</tr>
<tr>
<td>8</td>
<td>1 -1 -1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1</td>
</tr>
<tr>
<td>9</td>
<td>-1 1 1 -1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1 1 1 -1</td>
</tr>
<tr>
<td>10</td>
<td>1 1 1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
<td>11</td>
<td>-1 -1 1 1 1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
<td>12</td>
<td>1 1 -1 1 1 1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
<td>13</td>
<td>1 -1 1 -1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
<td>14</td>
<td>-1 -1 1 -1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
<td>15</td>
<td>-1 -1 -1 -1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1</td>
</tr>
<tr>
<td></td>
<td>1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32</td>
</tr>
</tbody>
</table>
PSSS –BPSK/ASK option (15/32 bit/s/Hz) – Coding example
PSSS – BPSK/ASK option (15/32 bit/s/Hz) – Precoding

1. Align PSSS symbol maxima symmetrical to 0
2. Scale PSSS symbol to amplitude limit

Minimal Resolution after precoding: 5 bit

Note:
Higher resolution further improves performance, but does not limit interoperability.
PSSS Amplitude Histogram
With Precoding

17 levels -> 5 bit resolution
IEEE802.15.4-2003 2.4 GHz PHY – Rx architecture example (1/16 Bit/s/Hz)

Note:
Most existing IEEE802.15.4 2.4 GHz chips are build with $\geq 4$-bit ADCs
PSSS - 8 Times parallel 2.4 GHz PHY derivate –
Rx: Original O-QPSK / I/Q proposal (1/2 bit/s/Hz) –
Digital correlation example

Very low increase (< 5%) of power consumption possible for Rx mode

2x 32 bit correlators

Note: Most existing IEEE802.15.4 2.4 GHz chips are build with ≥ 4-bit ADCs
PSSS - 8 Times parallel 2.4 GHz PHY derivate –
Rx: Original O-QPSK / I/Q proposal (1/2 bit/s/Hz) –
Analog correlation example

Very low increase (< 5%) of power consumption possible for Rx mode

No ADCs vs. Halfrate

16 analogue integrate & dump,
approx. 5-10k gates reduction
(no 2x 4x32 bit correlators)

Note:
The Rx example architectures shown (digital, analog, FIR correlator) and the modulation variant can be freely combined
PSSS - 8 Times parallel 2.4 GHz PHY derivate –
Rx - BPSK/ASK option (15/32 bit/s/Hz) –
FIR filter correlation example

Very low increase (< 5%) of power consumption possible for Rx mode

Only single ADC vs. Halfrate
FIR filter (31 taps)
approx. 5-10k gates reduction vs. halfrate (no 2x 4x32 bit correlators)
Linearity –
Transfer function for non-linear system simulated
Linearity – Simulation results

20% non-linearity

10% non-linearity

5% non-linearity

0% non-linearity

Detection threshold (for '0' or '1' data bits)