IEEE P802.11
Wireless LANs

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| CC50 CR Prioritized EDCAs |
| Date: 2025-05-13 |
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Abstract

This submission proposes the resolution to CID 214 received for CC50 for 802.11bn which was previously missed in document 11-25/627r13.

It also provides corrections to the text inconsistencies/bugs that were reported offline by various member since draft 0.3 release.

CID 214

# Revision information

The following is a summary of the important changes that occurred within each revision of this document:

|  |  |
| --- | --- |
| **Revision** | **Major changes** |
| 0 | Initial revision of the document using draft 0.3 as a baseline. Initial version contain changes vs baseline as follows: |
| 1 | Defined P-EDCA Operation Information field Highlighted new text with turquoise color |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **CID** | **Commenter** | **Comment** | **Proposed Change** | **Resolution** |
| 214 | Pei Zhou | There is current no definition for 'low latency' in 802.11 baseline. But there is 'Low Latency Indication' in 802.11bn draft 0.1 (see clause 37.16).Therefore, what does 'low latency' mean here? | Either add detailed defination for 'low latency' or just delete 'low latency' (if AC\_VO equals to low latency traffic). | Revised . Similarly to resolution ifor CID 3436, removed “low latency”Apply the same changes as CID 3436 in DCN 11-25/0627r13 |
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Reported issues:

**P119L52**

The RA field shall be set to the unicast MAC address with OUI 00:0F:AC and the remaining bits set by <ANA>

**Discussion:** ANA has assigned remaining bits, MAC address value is 00-0F-AC-47-43-00

**Proposed resolution: change text to “**The RA field shall be set to the unicast MAC address 00-0F-AC-47-43-00 set by ANA

**P119L33:**

QSRC[AC\_VO] is equal or greater than dot11PEDCARetryThreshold and PSRC[AC\_VO] is not greater than dot11PEDCAConsecutiveAttempt.

**Issue:** Highlighted text is a result on copy-paste error and should be changed as “is less than”.

**Discussion:**

With the current language, if dot11PEDCAConsecutiveAttempt is set to 1, a P-EDCA STA will be able to perform 2 transmission which is not the intention. At first DS-CTS transmission attempt, PSRC[AC\_VO] increase from zero to 1, before attempting next DS transmission, a P-EDCA STA compare PSRC (1) with dot11PEDCAConsecutiveAttempt (1) -> RSRC(1) <= dot11PEDCAConsecutiveAttempt (1) and commence another DS-CTS transmission.

**Proposed change:** correct “not greater” with “less”

**P120L53-56**

Additionally, the EDCAF[AC\_VO] shall update the AIFSN, CWmin, and CWmax with the values in dot11EDCATable (dot11QAPEDCATable for the AP) and an operation of the EDCAF[AC\_VI], EDCAF[AC\_BE], EDCAF[AC\_BK] is resumed.

**Issue**: After P-EDCA STA exhausted allowed number of P-EDCA contention attempts, STA shall fall back to EDCA operation. The text mandate STA to update CWmin, CWmax, and AIFSN of EDCAF[AC\_VO] to be updated to the values from dot11EDCATable but it does not specify how CW[AC\_VO] is initialized. Text in P119L62 explain that CW[AC\_VO] is initialized to CWmin[AC\_VO] when STA initiates P-EDCA contention, but nothing is said about transition back to EDCA.

Similar issue is reported with lines P120L36

**Discussion:**

At a start of P-EDCA contention, CW for EDCAF[VO] is initialized to the CWmin[AC\_VO] which in turn initialized from Table 37-1. This values and values from dot11EDCATable can differ, so correct behavior is to initialize CW[AC\_VO] according to the parameters relevant to EDCA procedure when STA fall back to EDCA operations.

**Proposed change:**

Add sentence “and CW[AC\_VO] shall be set to the lesser of CWmax[AC\_VO] and 2QSRC[AC] × (CWmin[AC\_VO] + 1) – 1. (see 10.23.2.2 EDCA backoff procedure)

# Text to be adopted begins here:

***TGbn editor: please make changes to the following subclause:***

* **UHR Operation Element**

***TGbn editor: Please update UHR Operation Parameters field to add P-EDCA Enabled field as below***

The format of the UHR Operation element is shown in UHR Operation element format.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Element ID | Length | Element ID Extension | UHR Operation Parameters | Basic UHR-MCS And NSS Set | DPS Operation Parameters | NPCA Operation Parameters | P-EDCA Operation Parameters |
| Octets: | 1 | 1 | 1 | 2 | 4 | 0 or 3 | 0 or 3 | 0 or 3 |
| * UHR Operation element format
 |

The format of the UHR Operation Parameters field is shown in ﻿Figure 9-aa2 (UHR Operation Parameters field format).

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | B0 | B1 | B2 | B3 | B4 B5 | B6 Bx |
|  | DPS Enabled | NPCA Operation Information Present | DBE Enabled | P-EDCA Enabled | Reserved | Reserved |
| Bits: | 1 | 1 | 1 | 1 | 3 | Y |
| * **UHR Operation Parameters field format**
 |

The P-EDCA Enabled field indicates whether the UHR AP is P-EDCA operation is enabled at the AP transmitting this field. T1he P-EDCA Enabled field is set to 1 to indicate that P-EDCA operation is enabled and set to 0 otherwise.

The P-EDCA Operation Parameters field contains parameters for P-EDCA operations is defined in Figure9-aa3 (P-EDCA Operation Parameters field format).

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | B0 B3 | B4 B7 | B8 B11 | B12 B13 | B14 B15 | B16 B17 | B18 B23 |
|  | P-EDCA ECWmin | P-EDCA ECWmax | P-EDCA AIFSN | CW DS | P-EDCA PSRC threshold | P-EDCA QSRC threshold | Reserved |
| Bits: | 4 | 4 | 4 | 2 | 3 | 2 | 5 |

**Figure 9-aa5 ---P-EDCA Operation Parameters field format**

P-EDCA ECWmin, P-EDCA ECWmax and AIFSN fields indicate the CWmin, CWmax and AIFSN value that are used by a P-EDCA STA during P-EDCA contention as defined in 37.5 (Prioritized EDCA). The P-EDCA ECWmin, ECWmax fields encode the value of P-EDCa Cwmin and P-EDCA CWmax respectively in exponential form. P-EDCA ECWmin and P-EDCA ECWmax values are defined so that

P-EDCA CWmin=2P-EDCA CWmin ⎯ 1

P-EDCA CWmax=2P-EDCA CWmax ⎯ 1

Values greater than 3 are reserved, hence the minimum encoded value of P-EDCA CWmin and P-EDCA CWmax is 0, and the maximum is 7. Values of P-EDCA AIFSN field that are greater than 2 are reserved.

The CW DS field indicate the CWds value used for the randomization of the transmission slot of the DS-CTS frame. Value 3 is reserved. Value 0 indicate that randomization not enabled.

The P-EDCA PSRC threshold field indicates number of a maximum allowed consecutive DS-CTS transmissions. Value 0 and values greater than 4 are reserved.

The P-EDCA QSRC threshold field indicate the value of QSCR[AC\_VO] counter to be allowed to start P-EDCA contention. Value 0 is reserved.

37.5 Prioritized EDCA

Prioritized EDCA (P-EDCA) is an enhancement of the EDCA mechanism (see 10.23.2 (HCF contention based channel access (EDCA)) that reduces the access delay distribution tail for (#856, #1426, #3436, #214)AC\_VO traffic(#2378, #3250, #477, #3355, #1483). The use of P-EDCA by a UHR STA balances the impact on STAs that do not support(#479) P-EDCA by the rules and restrictions that are defined below. (#186, #478, #858, #879, #1044, #2379, #2545, #1858, #1816, #1427, #1488, #2966, #3315, #3354, #3356, #3966, #479)

(#857, #1387, #1805, #2380, #2381, #2382, #2383, #2384, #2385, #2386, #1484, #1490)A STA that has dot11PEDCAOptionActivated equal to true is called a P-EDCA STA and shall set the P-EDCA Support subfield of the UHR MAC Capabilities Information field of the UHR Capabilities element to 1, otherwise the STA shall set the P-EDCA Support subfield to 0.

An AP that has enabled P-EDCA operation shall set the P-EDCA Enabled field in UHR operation element to 1.

P-EDCA STAs shall maintain a P-EDCA station retry counter, PSRC[AC\_VO]. The initial value for PSRC[AC\_VO] shall be 0. PSRC[AC\_VO] shall be incremented by 1 with every transmission of the DSCTS frame. PSRC[AC\_VO] shall be set to 0 when QSRC[AC\_VO] is set to 0.

A P-EDCA STA may start a P-EDCA contention if all of the following conditions are satisfied:

* (#2644, # 2645, # 3944) P-EDCA is enabled by the AP in the BSS and the P-EDCA non-AP STA has notified the AP of its intent to use P-EDCA on the link.
* The P-EDCA STA has pending AC\_VO buffered traffic
* QSRC[AC\_VO] is equal or greater than dot11PEDCARetryThreshold and PSRC[AC\_VO] is less than dot11PEDCAConsecutiveAttempt

To start the P-EDCA contention, the P-EDCA STA shall transmit [#339] a Defer Signal CTS (DS-CTS) frame.

The DSAIFS[AC\_VO] is a duration derived from the relation:

DSAIFS[AC\_VO] = aSIFSTime + (AIFSN + DSr) × aSlotTime

where AIFSN is 2 and DSr is an integer value chosen randomly with a uniform distribution taking values in the range 0 to CWds[AC\_VO] for every transmission of DS-CTS frame. The transmission of the (#339)DSCTS frame shall occur at the DSAIFS[AC\_VO] slot boundary if the STA's CS mechanism (see 10.3.2.1 (CS mechanism)) determines that the medium is idle. The (#339)DS-CTS frame shall be transmitted in a non-HT PPDU or non-HT PPDU duplicate format, using 6 Mb/s data rate, and SCRAMBLER\_INITIAL\_VALUE is fixed. The RA field shall be set to the unicast MAC address 00-0F-AC-47-43-00 set by <ANA>, and the Duration field shall be set to the value of the P-EDCA contention duration in Table 37-1 (Default P-EDCA parameter set).

The P-EDCA contention shall start immediately after the end of the transmitted (#339)DS-CTS frame and shall follow the random backoff procedure defined in 10.23.2.4 (Obtaining an EDCA TXOP) except that:

* Only EDCAF[AC\_VO] shall be allowed to contend during the P-EDCA contention. Operation of the other EDCAFs is suspended.
* (#341)The EDCAF[AC\_VO] shall initialize AIFSN, CWmin, and CWmax with the values of PEDCA AIFSN, P-EDCA CWmin, and P-EDCA CWmax respectively. CW[AC\_VO] shall be initialized to CWmin[AC\_VO].
* The EDCAF[AC\_VO] shall set the backoff counter to an integer value chosen randomly with a uniform distribution taking values in the range 0 to CW[AC\_VO].

Table 37-1 (Default P-EDCA parameter set) defines the default P-EDCA parameter used by a P-EDCA STA when the AP does not advertise a P-EDCA parameter set for the P-EDCA contention, for the transmission of a DS-CTS frame, and for the conditions to start P-EDCA. If the AP advertises P-EDCA parameter set for the parameters in Table 37-1 (Default P-EDCA parameter set), then the P-EDCA STA shall update the P-EDCA parameter set to the most recent received P-EDCA parameter set.

A P-EDCA STA that initiates a TXOP (see 10.23.2.4) during a P-EDCA contention shall transmit an RTS frame as initial frame in the TXOP(#1486, #1487).

A P-EDCA STA that successfully (as defined in 10.23.2.2 EDCA Backoff procedure) delivered one or more pending MPDUs in a TXOP obtained during P-EDCA contention shall not start P-EDCA contention until conditions to start P-EDCA are satisfied. Additionally, the EDCAF[AC\_VO] shall update AIFSN, CWmin, and CWmax with the values in dot11EDCATable (dot11QAPEDCATable for the AP) and an operation of EDCAF[AC\_VI], EDCAF[AC\_BE], EDCAF[AC\_BK] is resumed. Additionally, CW[AC\_VO] shall be set to the lesser of CWmax[AC\_VO] and 2QSRC[AC] × (CWmin[AC\_VO] + 1) – 1. (see 10.23.2.2 EDCA backoff procedure)

NOTE 1—After successful delivery of one or more pending MPDUs the STA resets QSRC[AC\_VO], therefore

conditions to start P-EDCA contention are no longer satisfied.

**Table 37-1 — [#M341] Default P-EDCA parameter set**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| AC | P-EDCA CWmin | P-EDCA CWmax | P-EDCA AIFSN | P-EDCA contention duration | CWds | P-EDCA PSRC threshold | P-EDCA QSRC threshold  |
| AC\_VO | 7 | 7 | 2 | 97 µs | 0 | 1 | 2 |
| NOTE 1— The NAV set by the Duration field of the DS-CTS frame protects the medium for the maximum P-EDCA contention duration: aSifsTime + (AIFSN + CWMax) \* aSlotTime. Hence, the values relate as follows: 97 µs = 16 µs + (2 + 7) × 9 µs NOTE 2—The value of the P-EDCA contention duration is fixed and is not advertised by the AP |

A P-EDCA STA that participated in a P-EDCA contention but did not initiate a TXOP (see 10.23.2.4) during the P-EDCA contention or that initiated a TXOP but did not receive the CTS frame in response to the RTS frame used to initiate the TXOP may start another P-EDCA contention by sending the DS-CTS frame at DSAIFSN[AC\_VO] slot boundary if the STA's CS mechanism (see 10.2.3.1 (CS mechanism)) determines that the medium is idle, for up to dot11PEDCAConsecutiveAttempt. If PSRC[AC\_VO] reaches dot11PEDCAConsecutiveAttempt transmission attempts, the P-EDCA STA shall not attempt to start PEDCA contention until the QSRC[AC\_VO] counter is reset and all the conditions to start P-EDCA defined in this subclause are satisfied. Additionally, the EDCAF[AC\_VO] shall update the AIFSN, CWmin, and CWmax with the values in dot11EDCATable (dot11QAPEDCATable for the AP) and an operation of the EDCAF[AC\_VI], EDCAF[AC\_BE], EDCAF[AC\_BK] is resumed. Additionally, CW[AC\_VO] shall be set to the lesser of CWmax[AC\_VO] and 2QSRC[AC] × (CWmin[AC\_VO] + 1) – 1. (see 10.23.2.2 EDCA backoff procedure)

NOTE 2—The STA follows the EIFS, CTSTimeout, and NAVTimeout deferral rules before attempting to transmit a DSCTS to start a P-EDCA contention.

**Text to be adopted ends here.**

**SP: Do you agree** **to incorporate the proposed text changes for P-EDCA in 11-25/1224r0 to the latest TGbn draft?**