IEEE P802.11  
Wireless LANs

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| CC50 MAC CIDs in 9.4.1.85 | | | | |
| Date: 2025-07-22 | | | | |
| Author(s): | | | | |
| Name | Affiliation | Address | Phone | email |
| Liwen Chu  Abstract  This submission proposed text change in 9.4.1.85 Transmission of DRU in D0.3.  899, 2409, 3612, ~~2410,~~ 2643, 2939, 1040, 777, 2647, 2675, 3614  Revisions:   * Rev 0: Initial version of the document. | NXP |  |  | Liwen.chu@nxp.com |

Interpretation of a Motion to Adopt

A motion to approve this submission means that the editing instructions and any changed or added material are actioned in the TGbn Draft. This introduction is not part of the adopted material.

***TGbn Editor: Editing instructions preceded by “TGbn Editor” are instructions to the TGbn editor to modify existing material in the TGbn draft. As a result of adopting the changes, the TGbn editor will execute the instructions rather than copy them to the TGbn Draft.***

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| **CID** | **Clause** | **Page** | **Comment** | **Proposed Change** | **Resolution** |
| 899 | 9.4.1.85 | 57.51 | DPS shall be defined prior to be used in the section. | change sentence to : "The dynamic power save (DPS) Operation Parameters field is defined ..." | Accepted |
| 2409 | 9.4.1.85 | 57.51 | Reference to Figure 9-207p is incorrect | "The DPS Operation Parameters field is defined in Figure 9-207p" | Acceptd |
| 3612 | 9.4.1.85 | 57.51 | Figure 9-207 should be Figure 9-207p | As suggested | Revised  Discussion: Generally agree with the commenter.  See CID 2409 |
|  |  |  |  |  |  |
| 2643 | 9.4.1.85 | 58.01 | Resolve the granularity for DPS Padding Delay and the maximum value in the following - "The DPS Padding Delay field contains an unsigned integer, in TBD units, that indicates a delay between 0 and TBD &#956;s." | Please resolve the details for the DPS Padding Delay | Revised  Discussion: Generally agree with the comenter. The maximal value of the delay is 256us that is similar to EMLSR oeration. The unit is 4us.  TGbn editor: please make chages in 11-25/1090R2 with tag 2643. |
| 2939 | 9.4.1.85 | 58.01 | "is calculated as defined in 37.14 (Padding for an Initial Control Frame)." -- that subclause does not appear to define how this is calculated. Surely it's not something that's calculated, it's a property of the implementation? | As it says in the comment | Revised.  Discussion: generally agree with the commenter. The related text is remoed from the draft specification.  TGbn editor: please make chages in 11-25/1090R2 with tag 2939. |
| 1040 | 9.4.1.85 | 58.02 | Replace TBDs with implementable values. | Replacing DPS Padding delay units TBD with 10 usec, replace DPS Padding delay maximum TBD with 2.55 msec, replace DPS Transition delay units TBD with 10 usc, replace DPS Transition delay maximum TBD with 2.55 msec - remove the initial TBD from the second paragraph that starts on line 5. | Revised  Discussion: Generally agree with the comenter. The maximal value of the delay is 256us that is similar to EMLSR oeration. The unit is 4us.  TGbn editor: please make chages in 11-25/1090R2 with tag 1040. |
| 771 | 9.4.1.85 | 58.05 | The DPS Transition Delay field is not supported by any motion. | Please remove this field. | Rejected.  Discussion: the DPS operation will follow EMLSR rules to decide the switchfrom HC mode to LC mode where the DPS Transition Delay will be used. |
| 2647 | 9.4.1.85 | 58.05 | Resolve the granularity for DPS Transition Delay and the maximum value in the following - "[TBD] The DPS Transition Delay field indicates the minimum amount of time required by a DPS STA to transition from the higher capability mode to the lower capability mode. The DPS Transition Delay field contains an unsigned integer, in TBD units, that indicates a delay between 0 and TBD &#956;s." | Please resolve the details for the DPS Transition Delay | Revised  Discussion: Generally agree with the comenter. The maximal value of the delay is 256us that is similar to EMLSR oeration. The unit is 4us.  TGbn editor: please make chages in 11-25/1090R2 with tag 2647. |
| 2675 | 9.4.1.85 | 58.05 | it is not clear why DPS transition delay is needed since when a DPS STA in HC mode can always transmit LC mode. | provide justification or remove the field and associated text. | Rejected.  Discussion: the DPS operation will follow EMLSR rules to decide the switchfrom HC mode to LC mode where the DPS Transition Delay will be used. |
| 3614 | 9.4.1.85 | 58.05 | The meaning of the "[TBD]" lacks context here and in several places and should be deleted. | As suggested | Rejected.  Discussion: the DPS operation will follow EMLSR rules to decide the switchfrom HC mode to LC mode where the DPS Transition Delay will be used. |

*TGbe Editor: Please make the following changes in 9.4.1.85.*

9.4.1 Fields that are not elements

9.4.1.85 DPS Operation Parameters field

The DPS Operation Parameters field is defined in Figure 9-207 (DPS Operation Parameters field format).

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|  | B0 B5 | | B6 B7 | | B8 B13 | B14 B15 |
|  | DPS Padding Delay | | Reserved | | DPS Transition Delay | Reserved |
| Bits: | 6 | | 2 | | 6 | 2 |
|  | |  | | * DPS Operation Parameters field format | | |

The DPS Padding Delay field indicates the minimum MAC padding duration that is required by a DPS STA in an ICF to cause the STA to transition from the lower capability mode to the higher capability mode(#2939). The DPS Padding Delay field is in units of 4 µs (#2643, 1040) (#2643, 1040). Values greater than 63 are reserved.

The DPS Transition Delay field indicates the amount of time required by a DPS STA to transition from the higher capability mode to the lower capability mode. The DPS Transition Delay field is in units of 4 µs. Values greater than 63 are reserved. (#2647)