IEEE P802.11
Wireless LANs

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| Resolution-to-some-XDMG-CIDs |
| Date: 2020-06-21 |
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|  |  |  |  |  |

Abstract

This document proposes resolution to some SB1 CIDs. The resolutions are based on D3.3

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| 4238 | 3132.00 | 20.9.2.2.3 | "A value of 0 in the PPDU Type(#1379) field and a value of 0 in the Beam Tracking Request field indicate aBRP-RX PPDU(#1379)." is not clear. It might mean that either condition makes a PPDU into a BRP-RX PPDU, or that both conditions need to be met | Change to "A value of 0 in both the PPDU Type(#1379) field and the Beam Tracking Request field indicates aBRP-RX PPDU(#1379)." | Accept |
| 4239 | 3132.00 | 20.9.2.2.3 | "A value of 0 in the PPDU Type(#1379) field and a value of 0 in the Beam Tracking Request field indicate aBRP-RX PPDU(#1379)." is not clear. It might mean that either condition makes a PPDU into a BRP-RX PPDU, or that both conditions need to be met | Change to "A value of 0 in both the PPDU Type(#1379) field indicates aBRP-RX PPDU(#1379). A value of 0 in the Beam Tracking Request field indicates aBRP-RX PPDU(#1379)." | Revise: Change to "A value of 0 in both the PPDU Type(#1379) field and the Beam Tracking Request field indicates aBRP-RX PPDU(#1379)." |

***Editor: in P3126L28 change the text as follows:***

A value of 0 in both the PPDU Type(#1379) field and the Beam Tracking Request field indicates a BRP-RX PPDU(#1379).

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| 4463 | 3097.00 | 20.3.5.1 | "Tc (SC)" -- the "(SC)" is spurious | Delete the "(SC)". Also at 3462.61 | **Revise** |

Discussion

The correct resolution is to accept, however there are other issues in table 20-4

***Editor: Modify the following lines in table 20-4 (P3089)***

|  |  |
| --- | --- |
| Parameter | value |
| *Fc*: chip rate | 1760 MHz  |
| *Tc*: chip time | (#4504) 1 / *Fc* (~0.57 ns) |
| *Tseq* | (#4504) 128 × *Tc* (~72.7 ns) |
| *TSTF*: Detection sequence duration | (#4504) 17× *Tseq* (~1236 ns) |
| *TCE*: Channel Estimation sequence duration | (#4504) 9 × *Tseq* (~655ns) |
| *THEADER*: header duration | (#1180) 2 × aSCBlockSize × *Tc* (~0.582 μs) (#2018)NOTE—aSCGIBlockSize is definedin Table 20-30 (DMG PHY characteristics) |
|  |  |
|  |  |
| (#1348)*TSTF-CM*: control mode short training field duration | (#4504) 50 × *Tseq* (~3.636 μs) |
| (#1348)*TCE-CM*: control mode channel estimation field duration | (#4504) *TCE* (~655ns) |
| *TData* | (#1180)(*NBLKS* × aSCBlockSize +aSCGILength) × *Tc* NOTE—*NBLKS* is defined in 20.5.3.2.3.3(LDPC encoding process) (#1180)andaSCBlockSize and aSCGILength are defined(#4504)in Table 20-30 (DMG PHYcharacteristics). |

***Editor: Modify the following lines in table 24-4 (P3468):***

|  |  |
| --- | --- |
|  |  |
| *Fc*: chip rate | 880 MHz  |
| *Tc*: chip time | 1 / *Fc* (~1.14 ns) |
|  |  |
| *Tseq*: | 128 × *Tc* (~146 ns) |
| *TSTF:* Detection sequence duration | 18 × *Tseq* (~2618.2 ns) |
| *TCE:* Channel estimation sequence duration | 9 × *Tseq* (~1309.1 ns) |
| *THEADER*: header duration | 3 × 512 × *Tc* (~1.75 μs) |
| *~~F~~~~CCP~~~~:~~* ~~Control mode chip rate~~ | ~~880 MHz~~ |
| *~~T~~~~CCP~~~~:~~* ~~Control mode chip time~~ | ~~1.14 ns = 1/~~*~~FCP~~* |
| *TSTF-CP:* Control mode short training field duration | 50 *× Tseq* (~7.2727 μs) |
| *TCE-CP:* Control mode channel estimation field duration | 9 × *Tseq* (~1309.1 ns) |
| *TData* | (*NBLKS* × aSCBlockSize + aSCGILength) × *Tc*NOTE—*NBLKS* is defined in 20.5.3.2.3.3(LDPC encoding process).aSCBlockSize and aSCGILength are defined(#4504)in Table 20-30 (DMG PHYcharacteristics). |

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| 4692 | 20 | CID 2036 follow-up, are the 128s in Figures 20-4/8 correct | As it says in the comment | Reject – they are correct |
| 4693 | 24 | CID 2036 follow-up, are the 128s in Figures 24-2/5 correct? | As it says in the comment | Reject – they are correct |

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| 4714 | 3504.00 | 25.3.9.1 | Table 25-7---Fields in the CMMG SIG field needs the same changes as made under CID 1351. However Assaf reports that it "requires (a lot of) more work because the scrambling is not mentioned in the encoding process." | Ask Assaf to kindly to the more work | Revise |

***Editor: make the following changes to table 25-7***

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| --- | --- | --- | --- |
| **Bit** | **Fields** | **Number****of bits** | **Description** |
| B0–B6 | Scrambler Initialization | 7 | Bits X1-X7 of the initial scrambler state (see 25.3.7). |

**References:**