IEEE P802.11
Wireless LANs

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| TDD Slot Structure CIDs |
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Abstract

This submission generalizes the guard periods between TDD slots in the TDD Slot Structure elemnt to independent periodss with possibly different durations. For some use cases (e.g., asymmetric traffic between AP and non-AP STAs) a single parameter (GT2) results in wasted airtime and inefficient slot structure.

As part of the generalization, the following CIDs are also resolved: 3034, 3035, 3036, 3558 and 3635. All proposed edits are in reference to IEEE P802.11ay/D2.2 and 802.11REVmd D2.0.

|  |  |  |  |
| --- | --- | --- | --- |
| CID | Clause | Comment | Proposed change |
| 3034 | 9.4.2.266 | GT1, GT2, GT3 no default values | Add default values |
| 3035 | 9.4.2.266 | GT1 and GT3 - they look redundat. GT3=GT1 | Remove GT3 and mark it as GT1 |
| 3036 | 9.4.2.266 | How should GT1,2,3 be used?Are they linked to "10.36.6.5 Guard time"If yes - it should be stated.If not - text to explain how should be used | Add text that links GTx with the Guard Time defined in 10.36.6.5 |
| 3558 | 9.4.2.266 | GT2 separate between RX to TX transition and also between TX to TX and RX to RX transition. It is more likely that guard time for the above cases would be different (implementation and use case). | Consider to define GT1 for GT3 case as well and allocate GT3 for the RX to TX transition or define new GT for the above case |
| 3635 | 9.4.2.266 | "The GT1 Duration, GT2 Duration and GT3 Duration subfields indicate the durations, in microseconds, of the GT1, GT2 and GT3 guard times shown in Figure 117." The role of GT1, GT2, and GT3 is not explained. There is no rule or recommendation how to compute the guard times and the illustrative figure 117 is not normative definition. It is not clear why two guard times GT1 and GT3 are presented on the switch from TX to RX, however the same GT2 is used between RX's and TX's and on the switch form RX to TX. The RX to TX switch of one side is an opposite on the other side and vise versa. The TDD slot structure element does not specify RX or TX use of the TDD slots. Due to It may be impossible to deliver accurate timing using the TDD slot structure element if unknown number of RX/TX switches happens inside the TDD interval and different GT is needed for it. | Provide clear definition of the Guard times, what are rules or recommendations how to compute the parameters. The definition shall resolve the mentioned issues. Propose to define GT1 to accommodate differences in timing between transmitter and receiver, GT2 to compensate time for antenna configuration and GT3 for min Tx to Rx turnaround time (SIFS). Propose to define TDD interval as unidirectional. Submission will be provided |
|  |  |  |  |

**Proposed resolution 3034, 3035, 3036, 3558, 3635:** Revised.

**Discussion**

The TDD Slot Structre in 802.11ay Draft 2.2 assuems a uniform (fixed) guard period between TDD slots in a Service Period operating in TDD mode. This results in inefficient airtime usage when highly optimized slot structures (i.e., slot durations and gurad periods) can be designed to accommodate a given scenario.

One example is shown below. In this example longer (and possibly more) slots are used for the downlink traffic from the AP (a Distribution Node in the Distribution Network use case) to non-AP STAs (Client Nodes in the Distribution Network use case), compared to slots used for ulplink traffic. The guard periods between slots used by AP for transmission can be very small, as small as zero, when non-AP STAs are beem-steered towards the AP and spend sufficient time in receive mode, before and after the slot during which they receive traffic from AP.



We note that,

* Number of slots does not need to match the number of non-AP STAs in this example. Several non-AP STAs are served by allocating different slots to different STAs during different TDD intervals. In fact, slots are often much fewer, showing the need for a highly optimized TDD interval that serves a group of non-AP STAs at a time (from this view, a TDD interval functions the same as a beacon interval with slots serving as Service Periods).
* More complex slot structures are used in practice to serve a variety of applications and node types

We also note two timing parameters, time synchronization error, and propagation time were missing from the TDD Slot Structure element. These two parameters together guide a receiving STA to enter and exit receive mode at suitable times relative to TDD slot boundaries.

Outline of the change is as follows: Guard periods GT1, GT2 and GT3 are replaced by a list of TDD Slot start time and durations. Also, figures are updated wherever applicable.

***TGay Editor: Make the following edits to subclause 9.4.2.266 (P150)***

**9.4.2.266 TDD Slot Structure element**

The TDD Slot Structure element defines the structure of a TDD SP described in 10.40.6.2.2. The format of the TDD Slot Structure element is shown in Figure 88.



**Figure 88 —TDD Slot Structure element format**

The Element ID, Length and Element ID Extension fields are defined in 9.4.2.1.

The Slot Structure Control field is defined in Figure 89.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Allocation ID | Maximum Time Synchronization Error | Maximum Propagation Time | Reserved |
| Bits: | 4 | 4 | 4 | 19 |

**Figure 89 —Slot Structure Control field format**

The Allocation ID subfield is set to the same value of the Allocation ID subfield in Allocation Control field of the Extended Schedule element describing the TDD SP allocation.

The Maximum Time Synchronization Error subfield indicates the maximum time synchronization error, in microseconds, between a transmitter and receiver in either direction.

The Maxiumum Propagation Time subfield indicates the maximum propagation time for any PPDU transmission.

NOTE – Maximum Time Synchronization Error and Maximum Propagation Time are upper bounds decided by the AP or PCP based on anticipated BSS structure. These parameters together help a target STA decide when to transition in and out of receive mode relative to the boundaries of TDD slots during which the STA is expected to receive PPDUs. Specifically, receiver STA should expect to receive PPDUs intended for the STA as early as max(*p* – *e*, *e*) before the slot starting boundary, and the intended PPDUS to last as late as *p + e* after the slot trailing boundary, where *e* and *p* are the values of the Maximum Time Synchronization Error and Maximum Propagation Time fields.

The Slot Structure Start Time subfield indicates the lower 4 octets of the TSF timer at the start of the first TDD interval in which the slot structure takes effect.

The Number of TDD Slots per TDD Interval subfield indicates the number of TDD slots in each TDD Interval.

The Slot Structure field is defined in Figure 90. The size of this field is 4*M* octets, where *M* is equal to the value of the Number of TDD Slots per TDD Interval subfield.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | TDD Slot 1Start | TDD Slot 1Duration | … | TDD Slot MStart | TDD Slot MDuration |
| Octets: | 2 | 2 | … | 2 | 2 |

**Figure 90 —Slot Structure field format**

The TDD Slot *i* Start subfield, 1 ≤ *i* ≤ *M*, indicates the start time, in microseconds, of the ith TDD slot relative to the beginning of each TDD interval.

The TDD Slot i Duration subfield, 1 ≤ *i* ≤ *M*, indicates the duration, in microseconds, of the ith TDD slot in each TDD interval.

The Number of TDD Intervals subfield indicates the time duration the slot structure holds, in units of number of TDD intervals.

The TDD Interval Duration subfield indicates the TDD interval duration in microseconds.

***TGay Editor: Replace Figure 122 with the following: (P228)***



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(For example, a set of simplex Tx TDD slots followed by a set of simplex Rx TDD slots)

**Figure 122 —Example of a TDD SP**

***TGay Editor: Revise the first paragraph after Figure 122 as following (P228L19)***

The slot structure for TDD slots within a TDD SP are defined by the TDD Slot Structure element. A non-AP and non-PCP STA shall not transmit a TDD Slot Structure element. A DMG AP or DMG PCP shall transmit a TDD Slot Structure element to each non-AP and non-PCP DMG STA that is expected to transmit or receive during a TDD SP. TDD Slot Structure elements may be included in DMG Beacon or Announce frames transmitted by the DMG AP or DMG PCP. Upon reception of a TDD Slot Structure element corresponding to allocations identified by the Allocation ID subfield value within the element, a DMG STA shall adopt the TDD slot structure within the element for all the TDD SPs identified by the same Allocation ID subfield value at the time indicated by the value of the Slot Structure Start Time subfield in the element. From the time the DMG STA receives an updated TDD Slot Structure element until the TDD structure is adopted, the current TDD structure shall remain in effect. The repetition period for each TDD interval in a TDD SP from one BI to the next BI is a fixed number equal to the BI duration.

***TGay Editor: Modify the paragraph at P229L7 as following:***

The assignment of the TDD slots within a TDD SP is done through the TDD Slot Schedule element. Except for the transmission of a TDD Beamforming frame prior to association, a DMG STA shall not transmit during a TDD SP unless it receives a TDD Slot Schedule element that indicates it is assigned, by the DMG AP or DMG PCP, to at least one TDD slot within the TDD SP that has the Bitmap and Access Type Schedule field for the STA equal to TX. A DMG STA shall not transmit outside the boundaries of the TDD slot it is assigned to with Access Schedule field equal to TX. The DMG AP or DMG PCP shall transmit the TDD Slot Schedule element conveyed through an MLME-TDD-SLOT-SCHEDULE.request primitive to each DMG STA that is assigned to access the TDD SP; this transmission shall be done using an Announce frame or Association Response frame before the time indicated by the value of the Slot Schedule Start Time subfield within the element. Upon reception of a TDD Slot Schedule element corresponding to allocations identified by the Allocation ID subfield value within the element, a DMG STA shall adopt the schedule within the element at the time indicated by the value of the Slot Schedule Start Time subfield within the element.

***TGay Editor: Modify the paragraph at P229L22 as following:***

A TDD slot can be a simplex TDD slot, an unavailable TDD slot, or an unassigned TDD slot. TDD slots shall not overlap. A STA shall not transmit in an unassigned TDD slot or an unavailable TDD slot. RX and TX operations during a simplex TDD slot depend on the STA behavior indicated in the Bitmap and Access Type Schedule field defined in Table 23 as follows: