IEEE P802.11  
Wireless LANs

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| EDMG-Header-A Encoding and Modulation for EDMG SC mode A-PPDU | | | | |
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Abstract

This document proposes additional specification text for EDMG-Header-A encoding and modulation for EDMG SC mode A-PPDU transmission.

Encoding and modulation

*Change the 2nd paragraph as follows:*

For an EDMG SC mode PPDU or an EDMG OFDM mode PPDU, the EDMG-Header-A field is encoded and modulated using two SC blocks of 448 chips with 64 guard symbols. The bits are scrambled and encoded as follows:

* The input 112 header bits are appended with 16 HCS bits calculated as defined in 20.3.7.
* The header 128 bits (including CRC) are scrambled as described in 20.3.9, starting from the first bit using a continuation of the scrambler bit sequence from the L-Header.
* The scrambled bits are divided into two parts  and  of 64 bits each. Each part is encoded taking the following steps:
  + To each data word  or , append 440 zero bits  and 168 parity bits  to create a codeword , such that , parity bits are computed applying *LCW* = 672, *R* = ¾ LDPC matrix defined in 20.6.3.2.3.2
  + Remove zero bits and discard (puncture) the last 8 parity bits to create a codeword  of length 224 bits
  + Remove zero bits and discard (puncture) the last but one 8 parity bits to create a codeword  of length 224 bits and then XOR with a PN sequence that is generated from the LFSR used for data scrambling defined in 20.3.9. The LFSR is initialized to the all 1s vector.
  + Concatenate  and  to create the output codeword  of length 448 bits.
* The resulting codewords  for  and  of 448 bits each, are then modulated applying π/2-BPSK modulation as defined in 20.6.3.2.4.2. This creates two SC data blocks EDMG-Header-A1 and EDMG-Header-A2 respectively.
* Each of the resulting two SC data blocks is prepended with 64 guard symbols to create SC symbol blocks. The second SC data block EDMG-Header-A2 is appended with appropriate number of guard symbols as described in 30.5.8.2.

~~For an EDMG A-PPDU transmitted over a~~ *~~N~~~~CB~~* ~~× 2.16 GHz channel (2 ≤~~ *~~N~~~~CB~~* ~~≤ 4) in the EDMG SC mode, the first SC symbol block (EDMG-Header-A~~~~1~~~~) and the second SC symbol block (EDMG-Header-A~~~~2~~~~) of a EDMG-Header-A~~*~~iPPDU~~* ~~field (~~*~~i~~~~PPDU~~* ~~≥ 1) are each repeated as specified in 30.5.6; that is, each EDMG-Header-A~~*~~iPPDU~~* ~~field is encoded using the same procedure as that of the EDMG-Header-B field.~~

For an EDMG A-PPDU transmission, EDMG-Header-A encoding and modulation for an EDMG SC mode A-PPDU and an EDMG OFDM mode A-PPDU are specified in 30.5.7 and TBD, respectively.

For an EDMG control mode PPDU, the EDMG-Header-A uses and continues the DMG control mode modulation and encoding (20.4.3.2.3). The scrambler is used to generate the EDMG-Header-A and its initial state is the final state of the scrambler from the preceding L-Header field.

* 1. EDMG SC mode

*Insert the following new subclause after 30.5.6:*

* + 1. Encoding of EDMG-Header-A for EDMG A-PPDU transmission

The EDMG-Header-A field in the first EDMG PPDU in an EDMG SC mode A-PPDU (i.e., *iPPDU* = 1, where *iPPDU* is defined in 30.3.2.2) is encoded and modulated as specified in 30.3.3.3.2.4.

For the *iPPDU*th EDMG PPDU in the EDMG SC mode A-PPDU, where 2 ≤ *iPPDU* ≤ *NPPDU* (where *NPPDU* is defined in 30.3.2.2), the EDMG-Header-A field shall be encoded and modulated as follows:

* Definitions:

Let:

Let:

where:

* *s*1, *s*2, …, *s*N represent the output of the scrambler with initial seed value (11, 12, …, 17)
* *iSTS* represents the space-time stream index number
* Steps:
* The input 112 header bits are appended with 16 HCS bits calculated as defined in 20.3.7.
* The header 128 bits (including CRC) are scrambled as described in 20.3.9, starting from the first bit using a continuation of the scrambler bit sequence from data field of preceding EDMG PPDU in the EDMG SC mode A-PPDU
* The scrambled bits are divided into two parts **b1** = (*B*1, *B*2,…, *B*64) and **b2** = (*B*65, *B*66,…, *B*128) of 64 bits each. Each part is encoded taking the following steps:
* To each data word **b** = **b1** or **b** = **b2**, append 440 zero bits **0** = (01, 02,…, 0440) and 168 parity bits **p** = (*p*1, *p*2,…, *p*168) to create a codeword **c** = (**b**, **0**, **p**), such that , parity bits are computed applying *LCW* = 672, *R* = 3/4 LDPC matrix defined in 20.6.3.2.3.2.
* Remove zero bits and discard (puncture) the last 8 parity bits to create a codeword **cs1** = (*B*1, *B*2,…,*B*64, *p*1, *p*2,…, *p*160) of length 224 bits
* Remove zero bits and discard (puncture) the last but one 8 parity bits to create a codeword **cs2** = (*B*1, *B*2,…,*B*64, *p*1, *p*2,…, *p*152, *p*161, *p*162,…, *p*168) of length 224 bits.
* Concatenate **cs1** and **cs2** to create the output codeword **cs** = (**cs1**, **cs2**) of length 448 bits.
* Generate codeword **d1*iSTS*** for each space-time stream *iSTS* for **b1** by XORing each corresponding bit of codeword **cs** and vector **s1*iSTS***.
* Generate vodeword **d2*iSTS*** for each space-time stream *iSTS* for **b2** by XORing each corresponding bit of codeword **cs** and vector **s2*iSTS***.
* For a 2.16 GHz channel transmission, the resulting codewords, **d1*iSTS*** and **d2*iSTS*** of 448 bits each, are modulated using π/2-BPSK modulation as defined in 20.6.3.2.4.2. This creates two SC data blocks EDMG-Header-A1*iSTS* and EDMG-Header-A2*iSTS* of length 448 chips for the *iSTS*th space-time stream.

Each of the resulting two SC data blocks is prepended with 64 guard symbols to create SC symbol blocks. The second SC data block, EDMG-Header-A2*iSTS*, is appended with approproate number of guard symbols as described in 30.5.8.2.2.2.

* For a *NCB* × 2.16 GHz channel transmission, where 2 ≤ *NCB* ≤ 4, each of the resulting SC data block is defined as:
* [EDMG-Header-A*jiSTS*, EDMG-Header-A*jiSTS*] for *NCB* = 2
* [EDMG-Header-A*jiSTS*, EDMG-Header-A*jiSTS*, EDMG-Header-A*jiSTS*] for *NCB* = 3
* [EDMG-Header-A*jiSTS*, EDMG-Header-A*jiSTS*, EDMG-Header-A*jiSTS*, EDMG-Header-A*jiSTS*] for *NCB* = 4
* where *j* = 1, 2

Each SC data block is prepended with a guard symbols. The second SC block, EDMG-Header-A2*iSTS*, is appended with appropriate umber of guard symbols as described in 30.5.8.2.3.

The content of EDMG-Header-A field in the *iPPDU*th EDMG PPDU in a *NCB* × 2.16 GHz channel (1 ≤ *NCB* ≤ 4) shall be identical on all space-time streams in the *NCB* × 2.16 GHz channel.

**References:**

1. Draft P802.11ay\_D0.5

**Straw Poll**

* Do you agree to include the EDMG-Header-A encoding and modulation for EDMG SC mode A-PPDU proposed in doc 11-17/1411r0 to the Draft amendment?