IEEE P802.11  
Wireless LANs

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| EDMG-Header-A encoding and modulation | | | | |
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Abstract

This document proposes specification text enhancements for subclause 30.3.3.3.2.4 (Encoding and modulation) describing EDMG-Header-A encoding and modulation process, [1].

*Editor: replace the subclause 30.3.3.3.2.4 (Encoding and modulation) in D0.5 with one proposed below, changes are highlighted by red*

**30.3.3.3.2.4 Encoding and modulation**

For an EDMG SC mode PPDU or an EDMG OFDM mode PPDU, the EDMG-Header-A field is encoded and modulated using two SC blocks of 448 chips with 64 guard symbols. The bits are scrambled and encoded as follows:

* The input 112 header bits are appended with 16 HCS bits calculated as defined in 20.3.7.
* The header 128 bits (including CRC) are scrambled as described in 20.3.9, starting from the first bit using a continuation of the scrambler bit sequence from the L-Header.
* The scrambled bits are divided into two parts  and  of 64 bits each. Each part is encoded taking the following steps:
  + To each data word  or , append 440 zero bits  and 168 parity bits  to create a codeword , such that , parity bits are computed applying *LCW* = 672, *R* = ¾ LDPC matrix defined in 20.6.3.2.3.2
  + Remove zero bits and discard (puncture) the last 8 parity bits to create a codeword  of length 224 bits
  + Remove zero bits and discard (puncture) the last but one 8 parity bits to create a codeword  of length 224 bits and then XOR with a PN sequence that is generated from the LFSR used for data scrambling defined in 20.3.9. The LFSR is initialized to the all 1s vector.
  + Concatenate  and  to create the output codeword  of length 448 bits.
* The resulting codewords  for  and  of 448 bits each, are then modulated applying π/2-BPSK modulation as defined in 20.6.3.2.4.2. This creates two SC data blocks EDMG-Header-A1 and EDMG-Header-A2 respectively.
* Each of the resulting two SC data blocks is prepended with 64 guard symbols to create SC symbol blocks. The second SC data block EDMG-Header-A2 is appended with appropriate number of guard symbols as described in 30.5.8.2.

symbol EDMG-Header-A1symbol EDMG-Header-A2PPDUPPDU

For an EDMG control mode PPDU, the EDMG-Header-A uses and continues the DMG control mode modulation and encoding (20.4.3.2.3). The scrambler is used to generate the EDMG-Header-A and its initial state is the final state of the scrambler from the preceding L-Header field.

**SP/M**: Do you agree to include the text proposed in 17/1300r0 (EDMG-Header-A encoding and modulation) into the 802.11ay draft spec?

**References:**

1. Draft P802.11ay\_D0.5