IEEE P802.11  
Wireless LANs

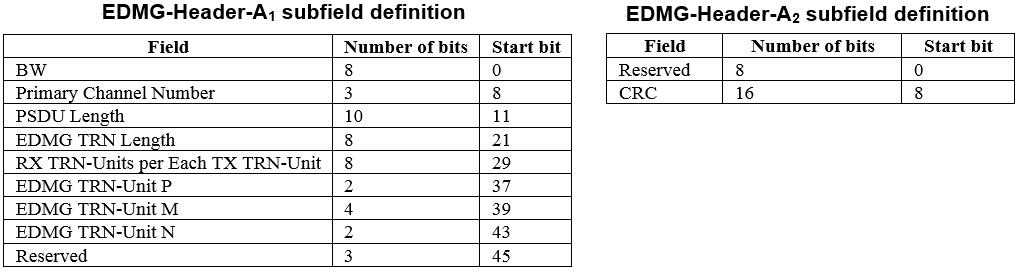
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| EDMG Control Mode Data Field | | | | |
| Date: 2017-03-02 | | | | |
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Abstract

This document suggests text that defines the processing steps (scrambling, encoding, modulation and spreading) of the data field of an EDMG control mode PPDU.

**Note:** The following definitions can be found in D0.2





**30.4.4.2 Data field**

~~The Data field consists of the payload data of the PSDU and is defined in 20.4.3.3~~

**30.4.4.2.1 General**The Data field consists of the payload data of the PSDU. The PSDU is scrambled, encoded, modulated and spread as described in the following subclauses.

**30.4.4.2.2 Scrambler**The operation of the scrambler is defined in 20.3.9. Bits x1, x2, x3, x4 of the scrambler shift register are initialized using the bits in the scrambler initialization bits from the L-Header, bits x5, x6, x7 are set to 1. The L-Header is scrambled starting from bit 5. The scrambling of the EDMG-Header-A continues the scrambling of the L-Header with no reset. The scrambling of the data field continues the scrambling of the EDMG-Header-A with no reset.

**30.4.4.2.3 Encoder**

The L-Header, EDMG-Header-A, and data field are encoded using an effective LDPC code rate less than or equal to 1/2, generated from the data PHY rate 3/4 LDPC parity check matrix, with shortening. The maximum number of data bits in each LDPC codeword is . The following steps are used for the encoding:

1. is the length of L-Header in octets. is the length of EDMG-Header-A1 in octets. The total (L-Header and EDMG-Header-A1) number of bits in the first LDPC codeword is .
2. is the length of EDMG-Header-A2 in octets. The EDMG-Header-A2 is transmitted in the second LDPC codeword.
3. The number of LDPC codewords is .
4. The number of bits in the second and any subsequent LDPC codeword (if present), except the last, is .
5. The number of data bits in the second LDPC codeword is .
6. The number of bits in the last LDPC codeword is .

NOTE—For example, if , then , , and . In the first LDPC block, the 88 bits consist of 40 L-Header bits along with 48 EDMG-Header-A1 bits. In the second LDPC block, the 150 bits consist of 24 EDMG-Header-A2 bits along with data bits.

**30.4.4.2.4 Modulation and Spreading**

The scrambled and coded bit stream is converted into a stream of complex constellation points by using the procedure defined in 20.4.3.3.4. The constellation points are then spread using the sequence Ga32(n), as defined in 20.4.3.3.5.

**Straw Poll**

Do you agree that the text in contribution 17/0277r0 shall be incorporated into the next draft 11ay specification?

**References:**