IEEE P802.11
Wireless LANs

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| 11ak PICS |
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Abstract

This document proposes initial PICS for 802.11ak to resolve CC17 CID 76 and corresponding changes to Clauses 8.4.2.171 and 9.42.

# Introduction

This document proposes initial PICS for 802.11ak to resolve CC17 CID 76 and corresponding changes to Clauses 8.4.2.171 and 9.42.

**Resolution:** Revised. As specified in submission 11-14/1438r2.

#### 8.4.2.171 GLK Capabilities element

***Remove “Extended SYNRA Support” from Figure 8-575b (GLK Capability Flags field format) and delete the first sentence after that figure.***

## 9.42 SYNRA address filtering operation

***Make the following changes:***

~~Values of the 2-bit SYNRA Type field are listed below.~~ Non-AP GLK STAs shall support the receipt of ~~type 0~~ SYNRAs but are not required to generate SYNRAs (since MPDUs to multiple receivers can always be sent with serial unicast) ~~and not required to support SYRNAs of non-zero type~~.

Values of the 2-bit SYNRA Type field are listed below.

|  |  |
| --- | --- |
| SYNRA Type | Description |
| 0 | AID bit array |
| 1 | Extended AID bit array |
| 2 | Extended AID list |
| 3 | Reserved |

If the SYNRA type is zero, the SYNRA control field is a bit array indicating which receivers in the AID range 1000 to 1021 are to accept the MPDU. B26 corresponds to AID 1000 and B47 corresponds to AID 1021. If the bit corresponding to an AID is 0, the STA having that AID for its association with the transmitter shall discard the MPDU. If the bit is a 1, the MPDU passes the address 1 filter.

If the SYNRA is type 3, the receiver ~~shall~~ discards the MPDU.

If the SYNRA type is 1 or 2, the SYNRA is called an extended SYNRA and the Control Field is considered to be composed of an 8-bit unsigned Extended SYNRA Size subfield ~~in bits B40 to B47~~ and an Extended SYNRA Second subfield as shown in Figure 9-91 Extended SYNRA Control subfields ~~consisting of bits B26 through B39~~. For extended SYNRA types, there is an Extended SYNRA Information field as described below. ~~If the receiver does not support extended SYNRAs, as indicated in its GLK Capabilities IE (see 8.4.2.171), it shall discard the MPDU.~~

Extended SYNRA Size subfield

 B25 B39 B40 B47

Bits: 14 8

 **Figure 9-91 – Extended SYNRA control subfields**

Extended SYNRA Second subfield

If the SYNRA type is 1, the Extended SYNRA Information is a ~~bit~~ vector of bits representing AIDs whose length in octets is equal to the Extended SYNRA Size subfield. This size may be zero, in which case all receivers discard the MPDU. If this size is non-zero, bit 0 of the vector represents the ~~16-bit~~ 14-bit AID (see 8.4.1.8) ~~with~~ contained in the 14-bit Extended SYNRA Second subfield ~~in the 14 LSBs and the 2 MSBs set to 1~~. Subsequent bits of the vector represent ~~a similar~~ AIDs formed by ~~but with 14 LSBs set to~~ the sum of the bit ~~number~~ index and the Extended SYNRA Second subfield treated as an unsigned integer. If the bit corresponding to an AID is 0, the station with that AID assigned to its association with the transmitter discards the MPDU. If the bit is a 1, the MPDU passes the address 1 filter.

If the SYNRA type is 2, the Extended SYNRA Information is a sequence of ~~an octet vector, each~~ ~~pair of~~ two-octet~~s~~ elements ~~being~~ each element containing an AID in the 14 LSBs. In this case, the Extended SYNRA Size subfield is the number of ~~pairs of octets~~ elements and only bit B25 of the Extended SYNRA Second subfield is used; bits B26 through B39 are ignored. If a receiver’s association with the transmitter is indicated by an AID in the ~~octet pair vector~~ sequence and B25 is 1, the receiver ~~shall~~ discards the MPDU. If a receiver’s association with the transmitter is not indicated by any AID in the octet pair vector and B25 is 0, the receiver ~~shall~~ discards the MPDU. If neither of these conditions applies, the MPDU passes the address 1 filter.

### B.4.3 IUT configuration

***Add the following entry:***

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |
|  | Item | IUT configuration | References | Status | Support |  |
|  | CF32 | GLK enabled STA | 10.45 (GLK Operation) | (NOT CF31):O | Yes **◻**︎ No ◻ N/A ◻ |  |
|  |  |  |  |  |  |  |

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#### B.4.4.2 MAC frames

***Add the following entries:***

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| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
|  | Item | MAC frame | References | Status | Support |  |
|  | FT43 | LPD MSDU | 5.1.4 (MSDU format) | O.1 | Yes **◻**︎ No ◻ N/A ◻ |  |
|  | FT44 | EPD MSDU | 5.1.4 (MSDU format), 10.46 (EPD Operation) | O.1 | Yes **◻**︎ No ◻ N/A ◻ |  |
|  | FR44 | LPD MSDU | 5.1.4 (MSDU format) | FT43:M | Yes **◻**︎ No ◻ N/A ◻ |  |
|  | FR45 | EPD MSDU | 5.1.4 (MSDU format), 10.46 (EPD Operation) | FT44:M | Yes **◻**︎ No ◻ N/A ◻ |  |
|  |  |  |  |  |  |  |

#### B.4.4.4 MAC addressing functions

***Add the folliwng entries:***

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
|  | Item | MAC Address function | References | Status | Support |  |
|  | AD12 | Receive SYNRA | 9.42 (SYNRA address filtering operation) | (CF32 AND NOT CF1):M | Yes **◻**︎ No ◻ N/A ◻ |  |
|  | AD13 | Transmit SYNRA | 9.42 (SYNRA address filtering operation) | (CF32 AND NOT CF2.1):O | Yes **◻**︎ No ◻ N/A ◻ |  |
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