

Field Measurements of 2x2 MIMO Communications

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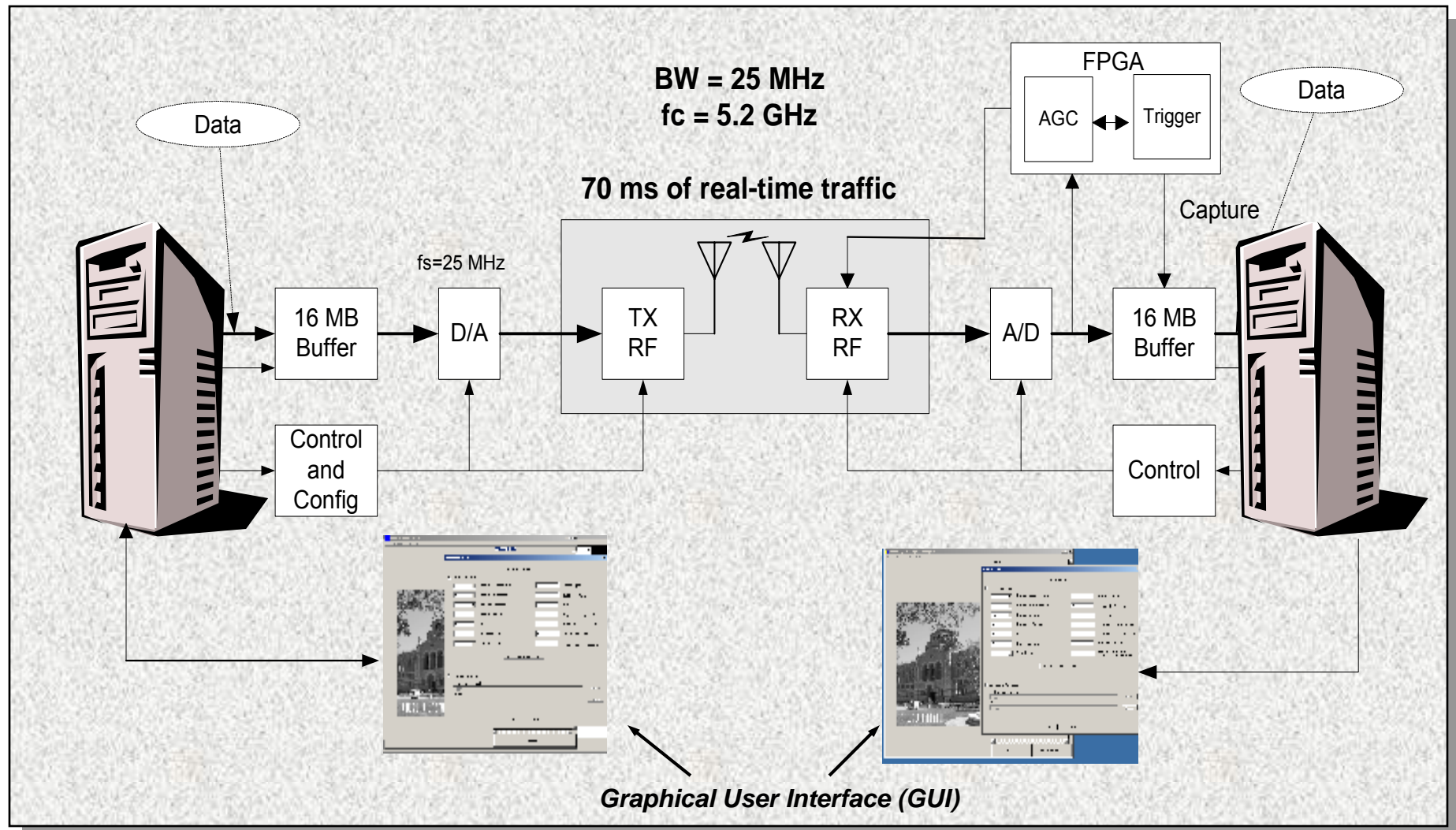
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Overview

- Testbed Overview
- Loss Due to IQ mismatch & phase noise
- Measurement Results
- MIMO Decoder ASIC

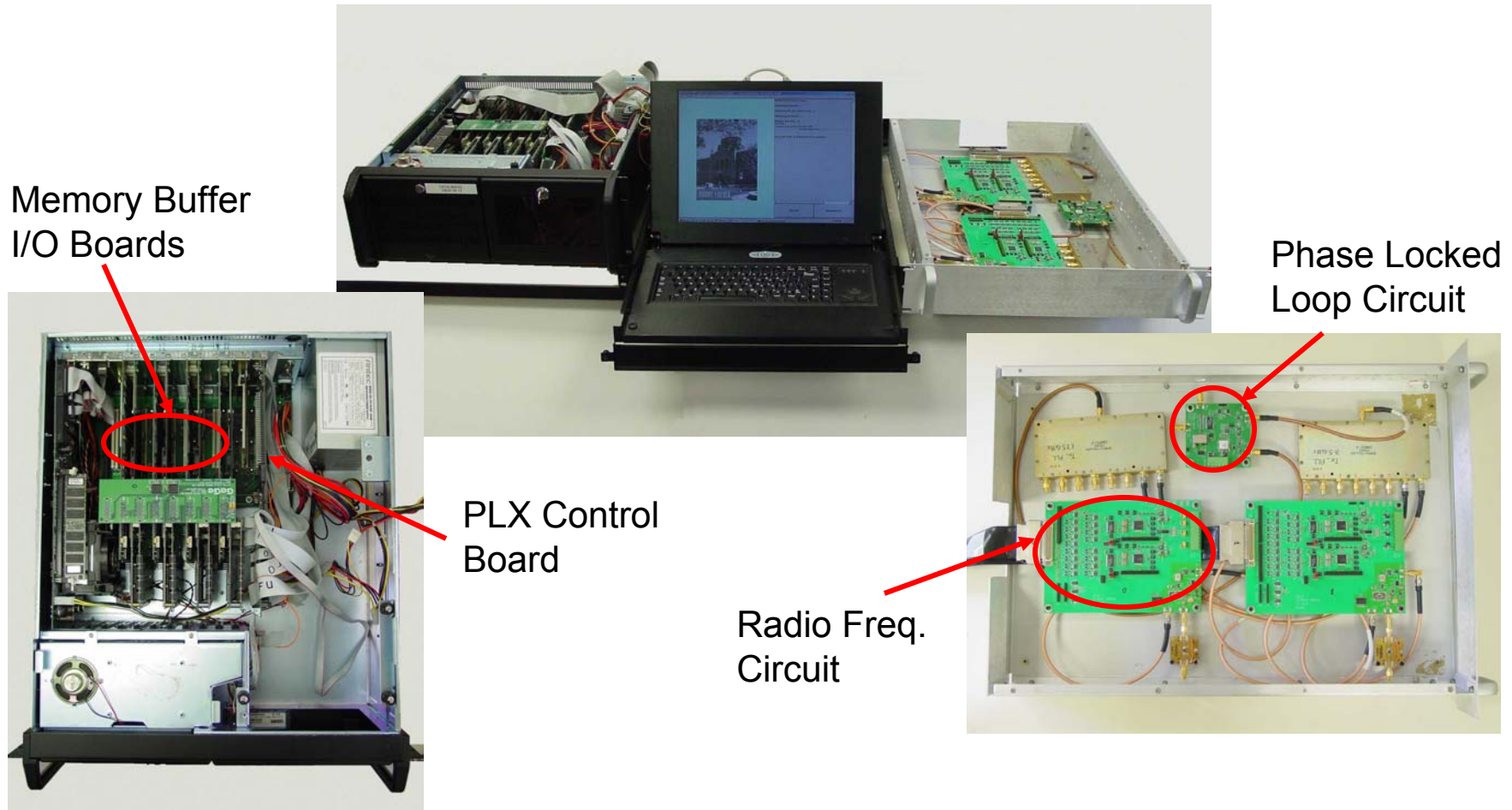
MIMO OFDM Testbed Overview

Top Level Functional Diagram

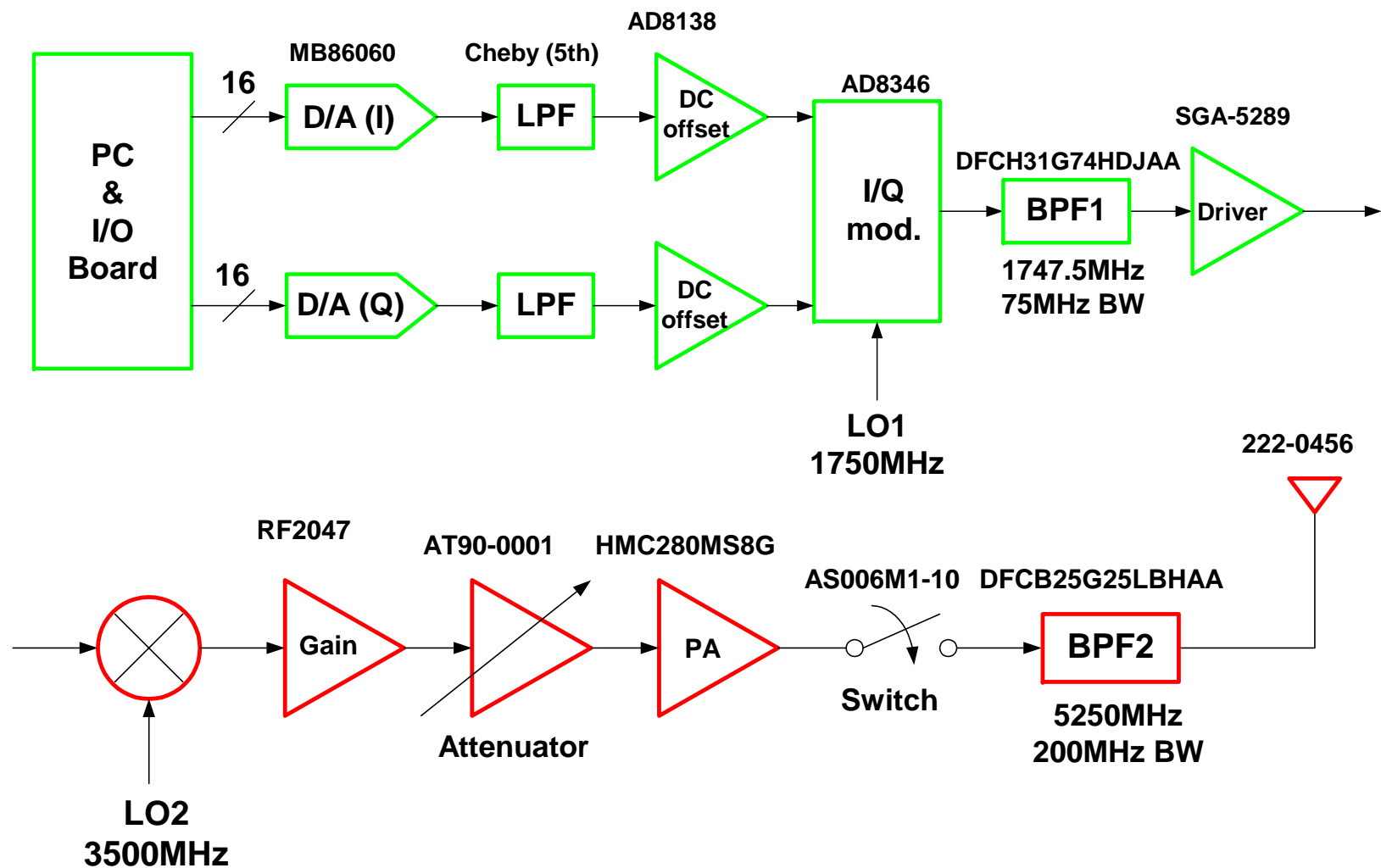


Testbed Components

UCLA Phase-2 2x2 MIMO Testbed

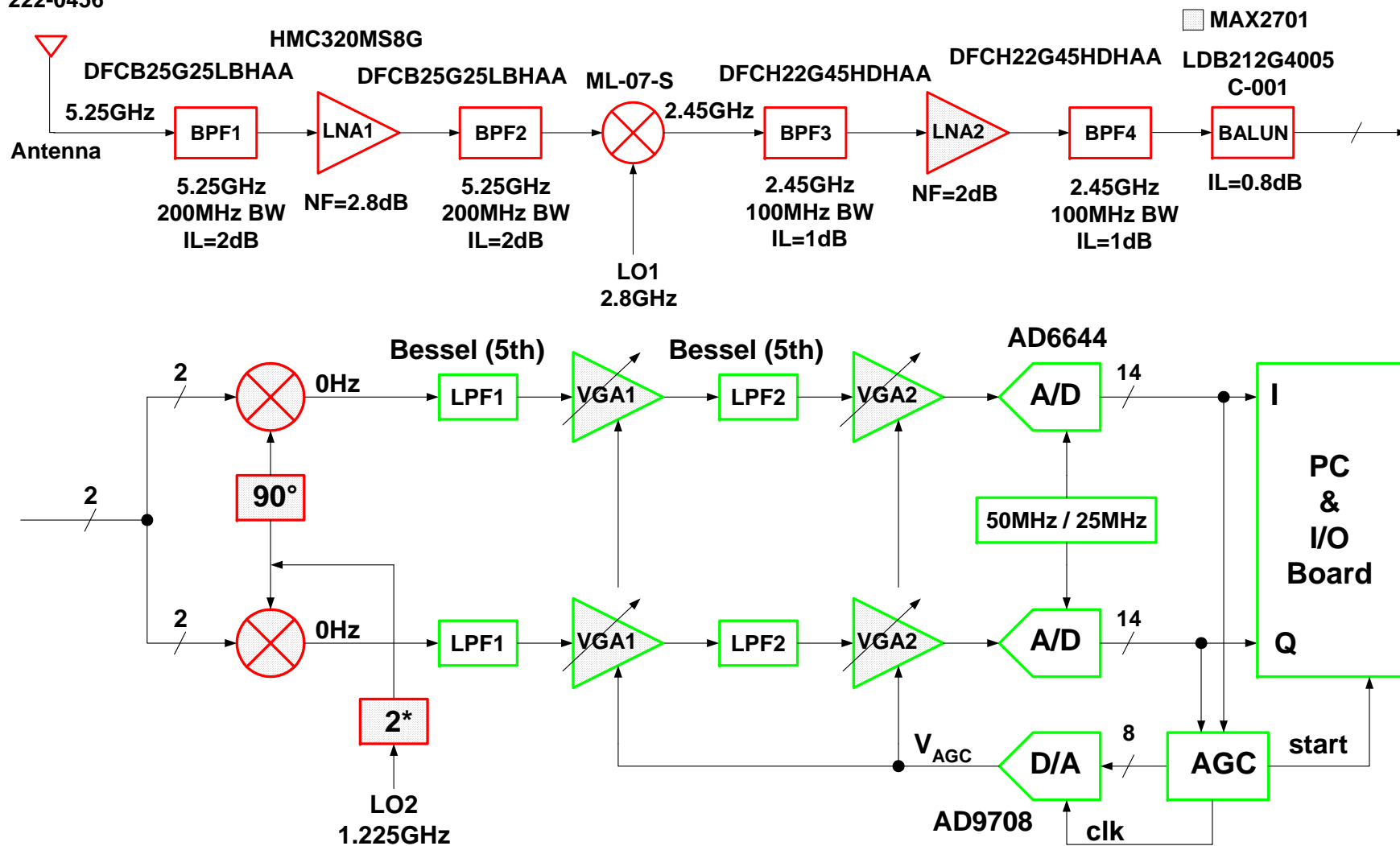


TX 2-Step RF Up-conversion

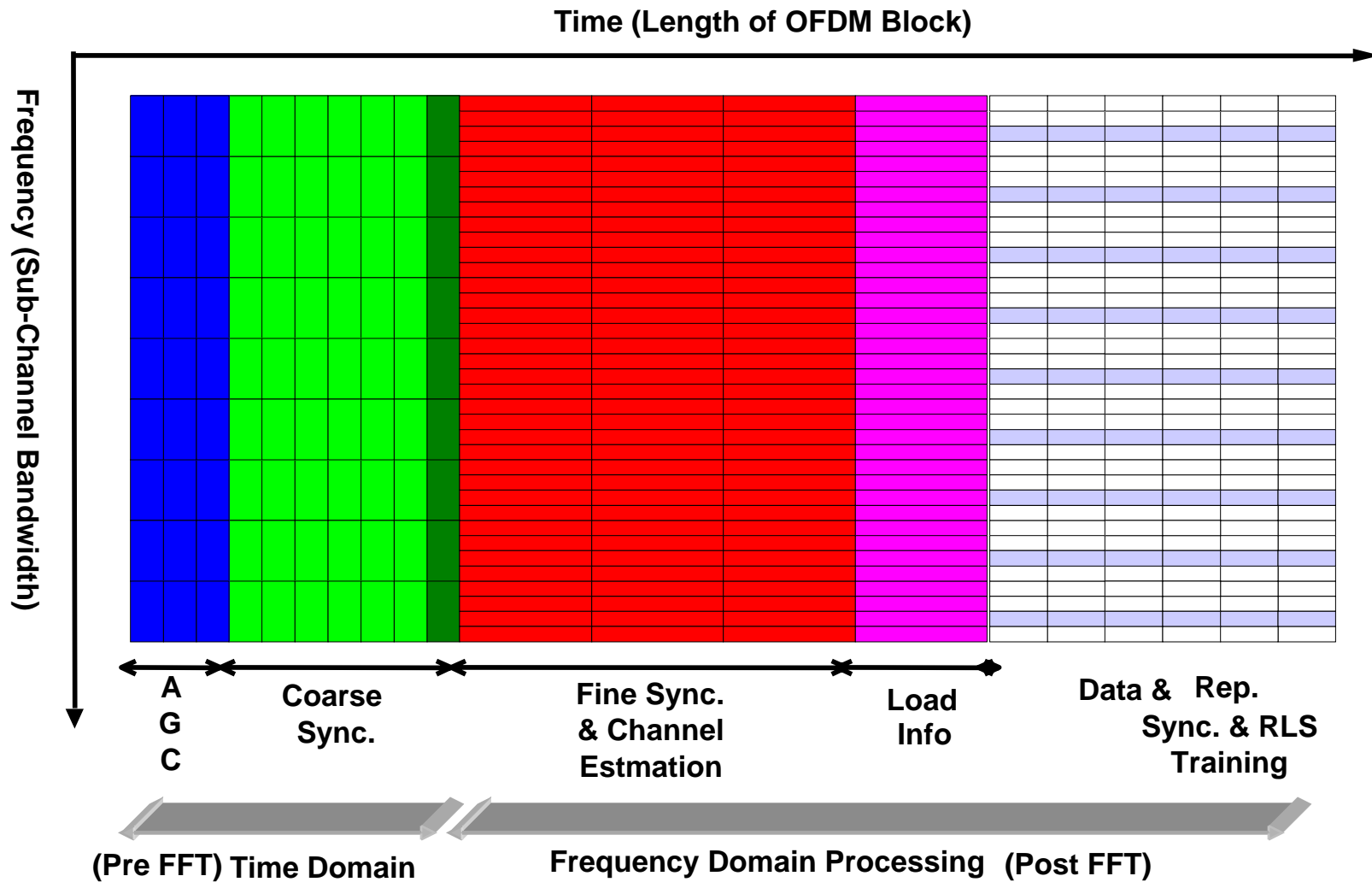


RX 2 step down-conversion

222-0456

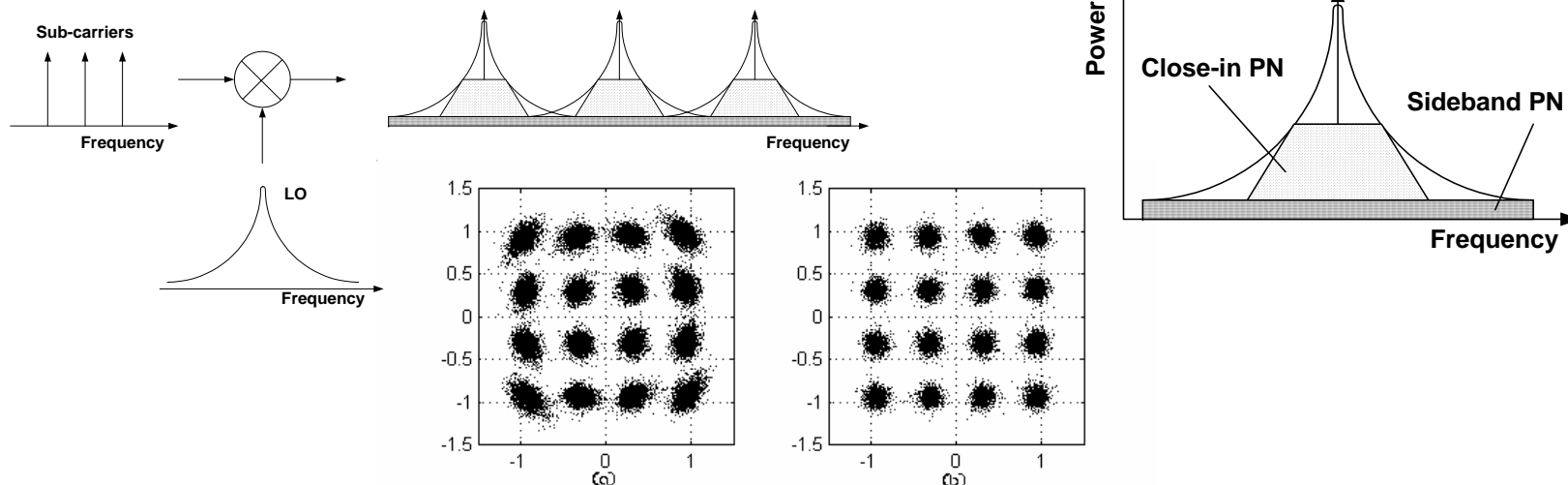


Packet Structure



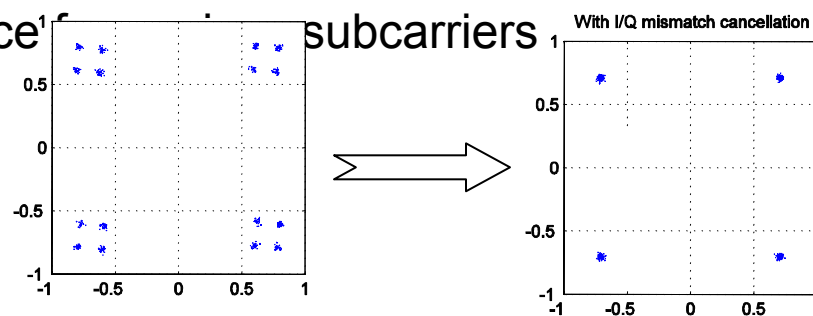
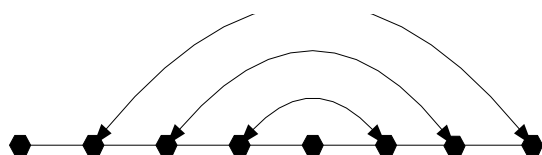
2 Major Impairments: Phase Noise & IQ Mismatch

Phase noise mitigation is critical to OFDM

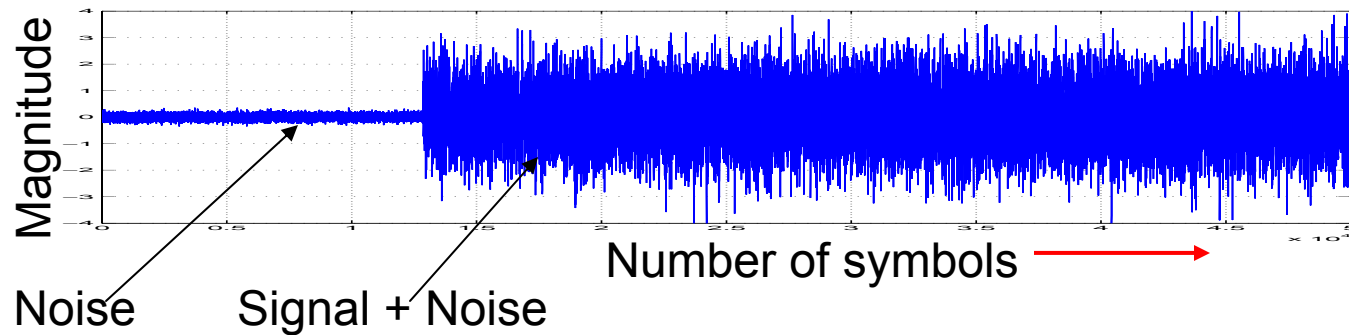


IQ mismatch, gain and phase, is present in all practical RF circuits

- I/Q mismatch causes interference

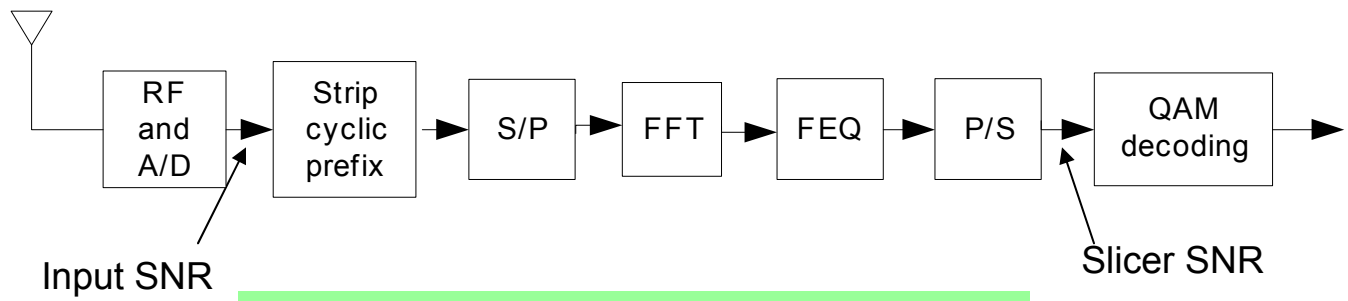


Calibration Metrics



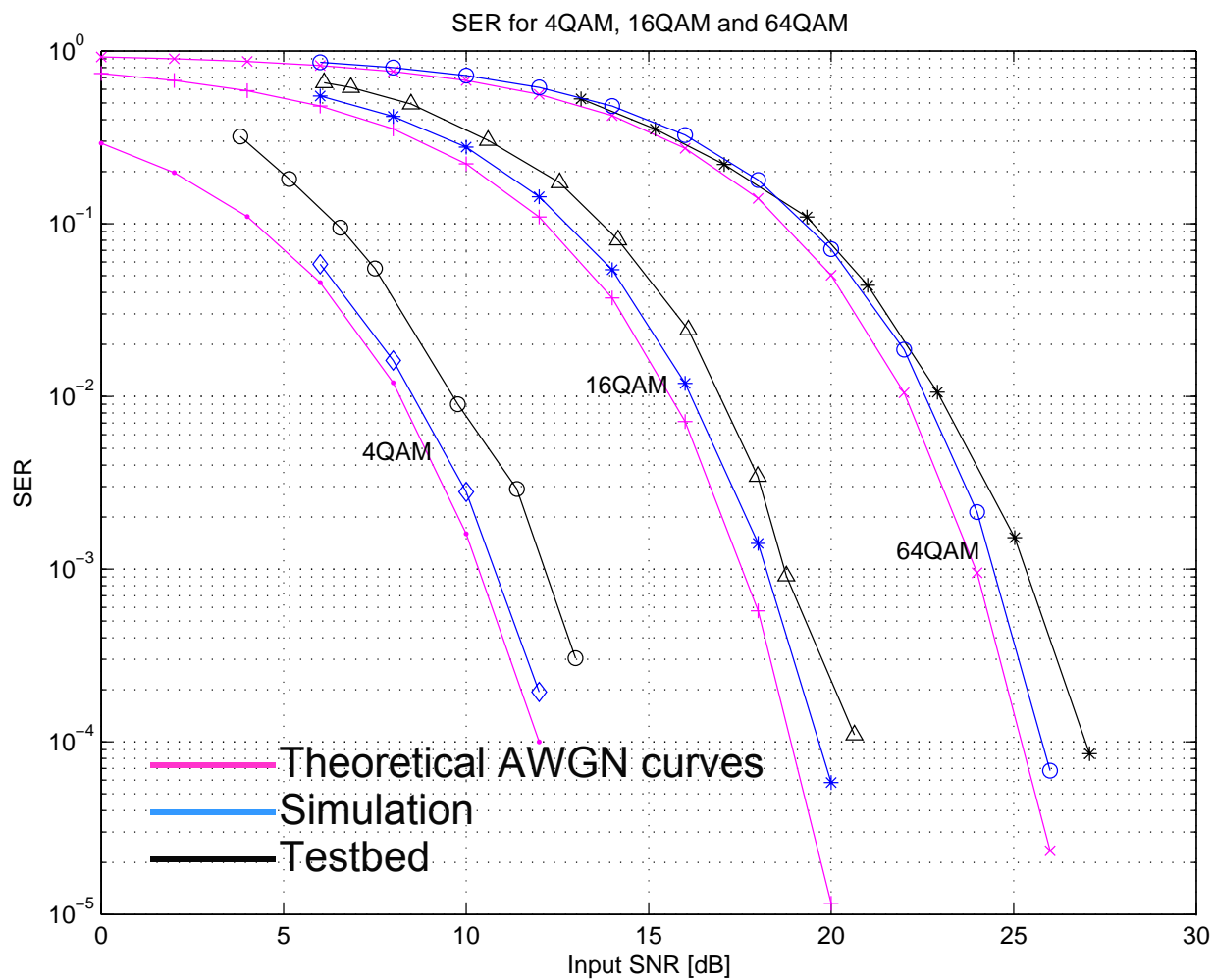
Calculated in the frequency domain

$$InputSNR = 10\log_{10}\left(\frac{(Signal + Noise) Energy}{Noise Energy} - 1\right)$$

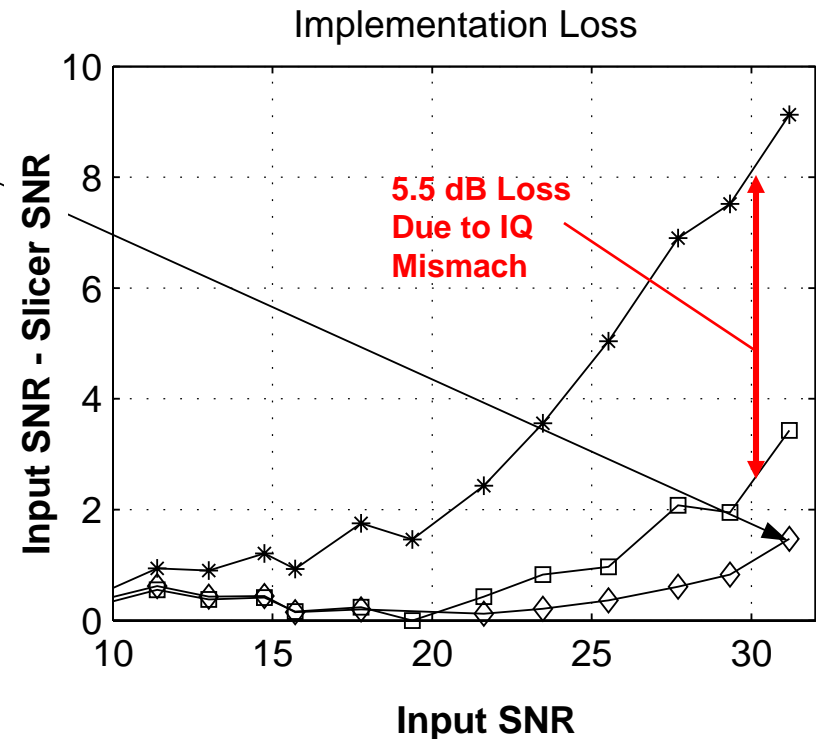
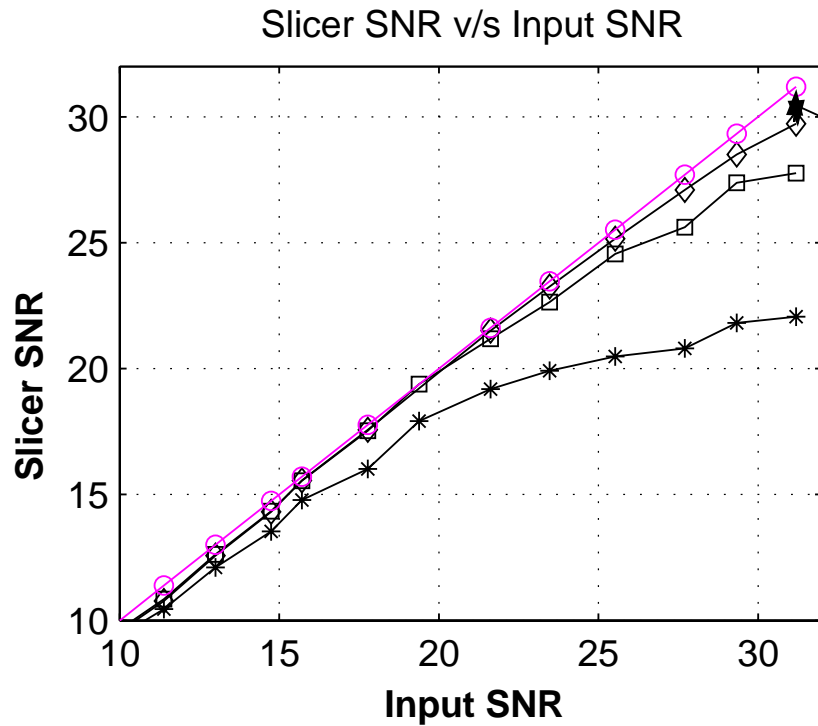


Implementation Loss = Input SNR - Slicer SNR

SER in Perfect Timing Mode



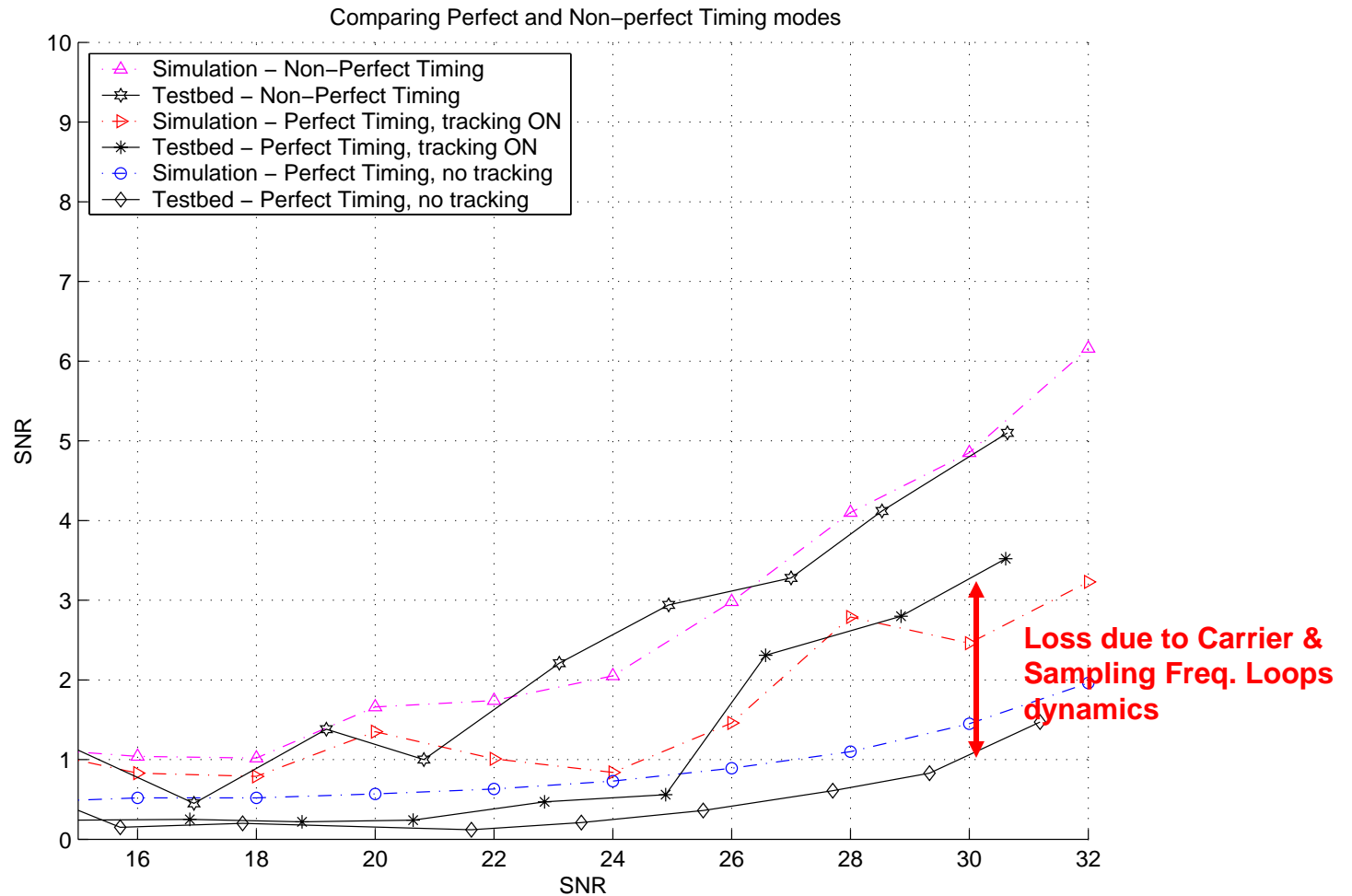
Testbed Calibration in Perfect Timing Mode



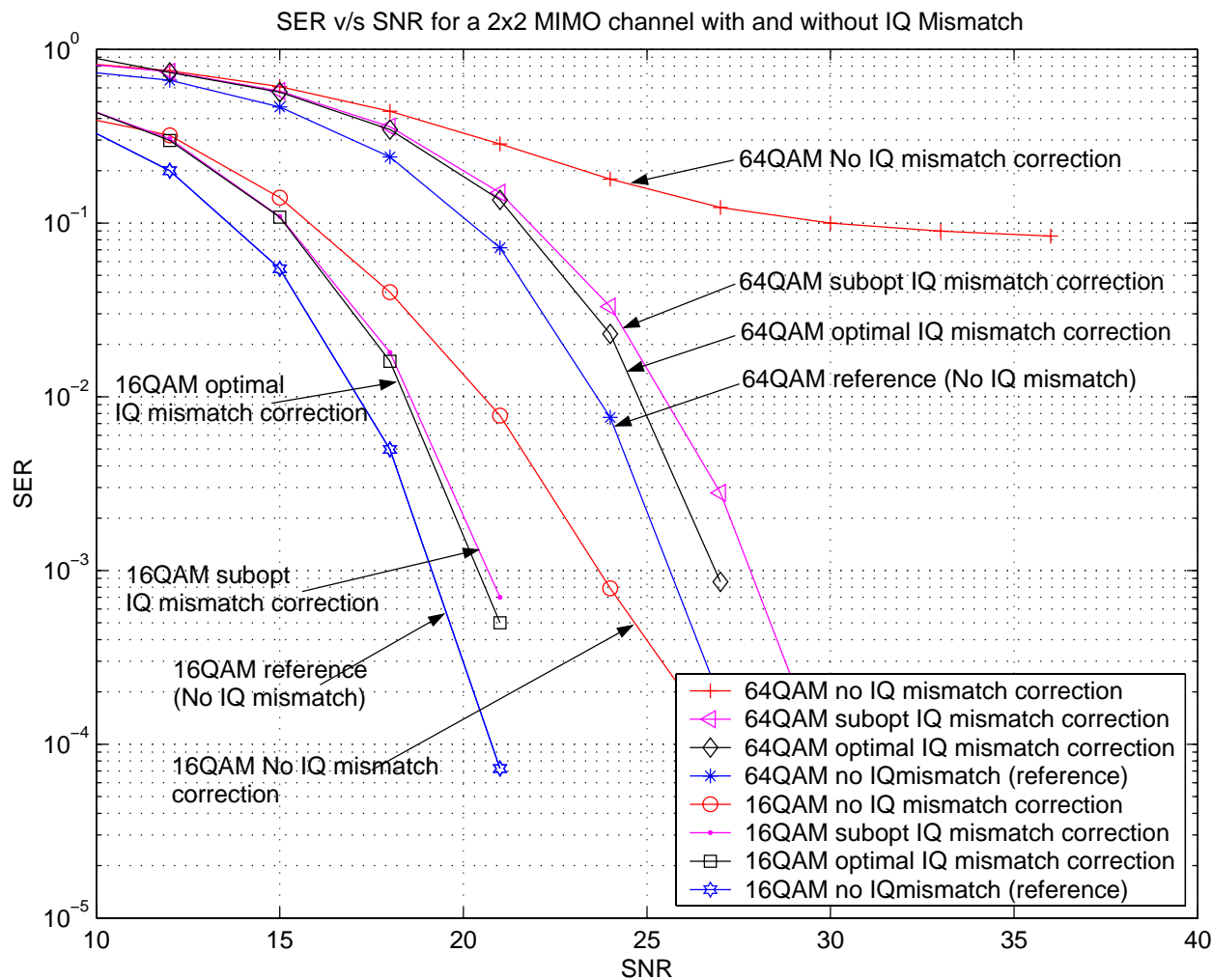
Comparing I/Q mismatch and Phase Noise Cancellation schemes on the testbed in perfect timing mode

- Reference
- * No I/Q mismatch cancellation, no Phase Noise cancellation
- With I/Q mismatch cancellation, no Phase Noise cancellation
- ◇ With I/Q mismatch cancellation, with Phase Noise cancellation

Implementation loss under non-perfect timing



Simulated Performance of MIMO-OFDM with and w/o I/Q Mismatch Cancellation



IQ gain mismatch
 Tx1 - (0.75,0.90)
 Tx2 - (0.85,0.95)
 Rx1 - (0.85,1.00)
 Rx2 - (0.90, 0.85)

IQ phase mismatch
 6 degrees at both the receivers

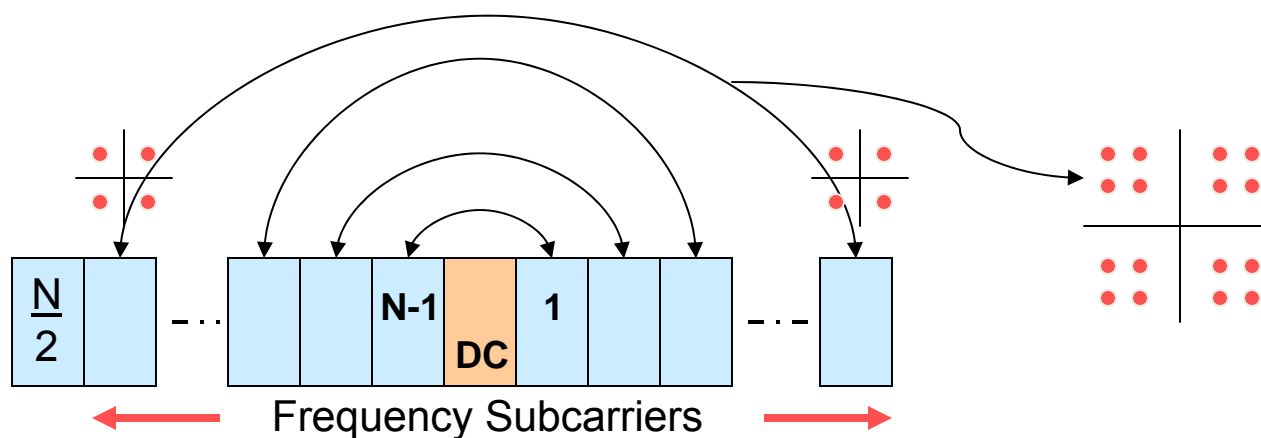
MMSE IQ Mismatch Canceller

I/Q mismatch in MIMO-OFDM systems

- I/Q mismatch is caused by an imbalance on the I-rail and Q-rails. This imbalance could be gain, delay or phase.
 - **Gain mismatch** occurs when the amplifiers on I-rail and Q-rail have different gains.
 - **Delay mismatch** occurs when the propagation delays on the two rails are different due to trace mismatches, different D/A skews, etc.
 - **Phase mismatch** occurs when the sinusoids used in the I/Q modulators and demodulators are not offset by 90 degrees.
- I/Q mismatch can be categorized as frequency independent or frequency dependent.
 - Gain and phase mismatches cause frequency independent I/Q mismatch.
 - Delay causes frequency dependent I/Q mismatch with distortion increasing on the high frequency subcarriers.

Effect of I/Q mismatch in an OFDM system

I/Q mismatch causes interference from the conjugate of the data on the frequency mirror sub-carrier.



$$\tilde{Y}(k) = \left[\frac{A(k) + B(k)}{2} \right] X(k) + \left[\frac{A(k) - B(k)}{2} \right] X^*(N - k)$$

I/Q delay mismatch

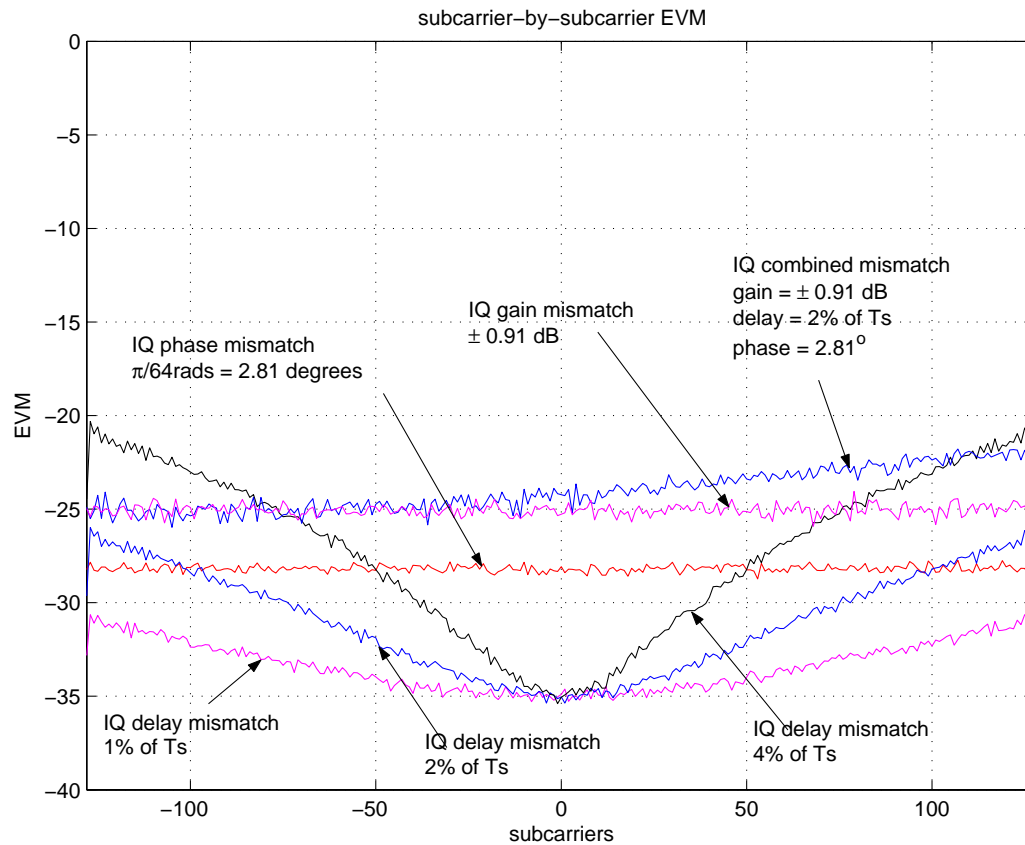
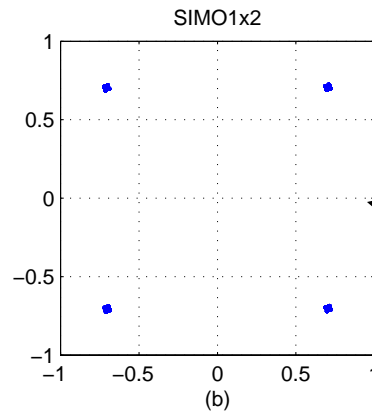
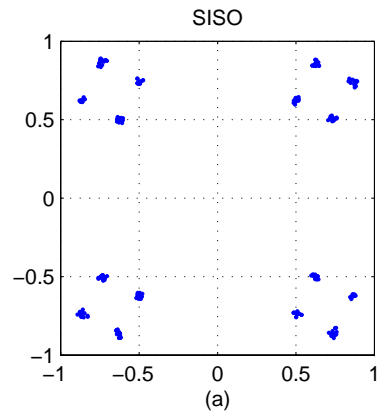


Image suppression

IQ mismatch	Min	Average
1% of Ts	-37.2 dB	-41.5 dB
2% of Ts	-31.3 dB	-35.5 dB
4% of Ts	-25.3 dB	-29.4 dB
2.81° phase	-32.19 dB	-32.19 dB
0.91dB gain	-25.57 dB	-25.57 dB

Image suppression is measured by transmitting data on half the subcarriers and measuring the image strength on the mirror frequencies

Effect of I/Q mismatch on a 4-QAM Constellation



Receive diversity helps with IQ mismatch. SIMO1x2 shows good improvement without any I/Q mismatch cancellation algorithms

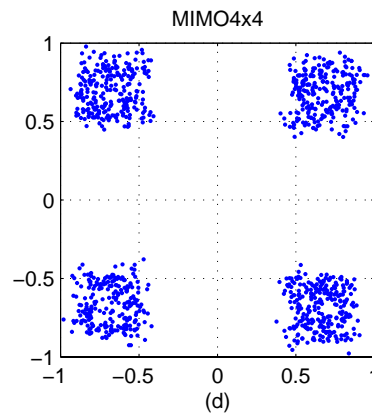
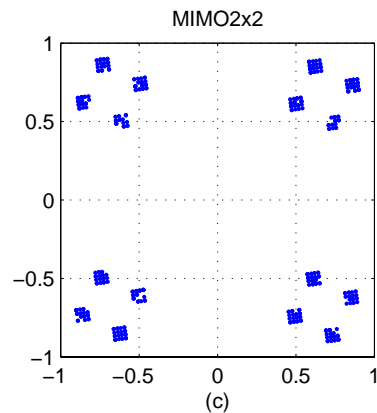
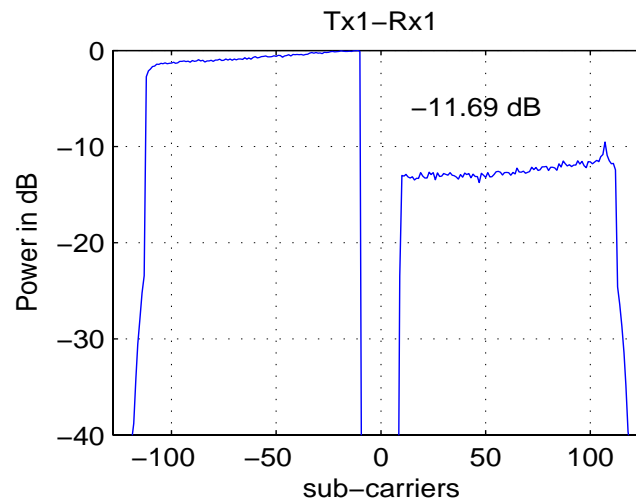
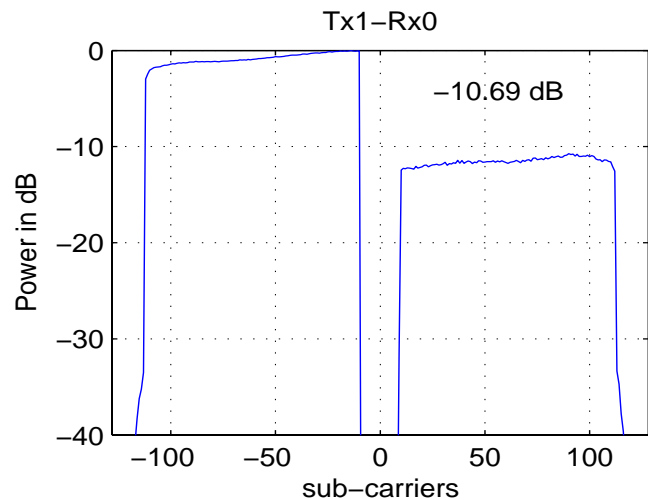
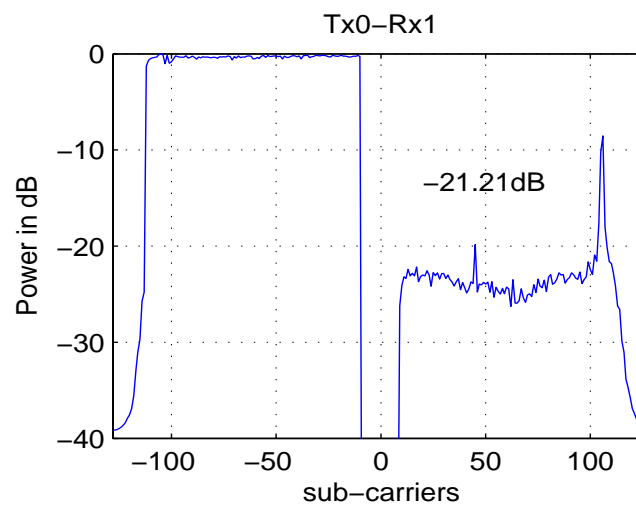
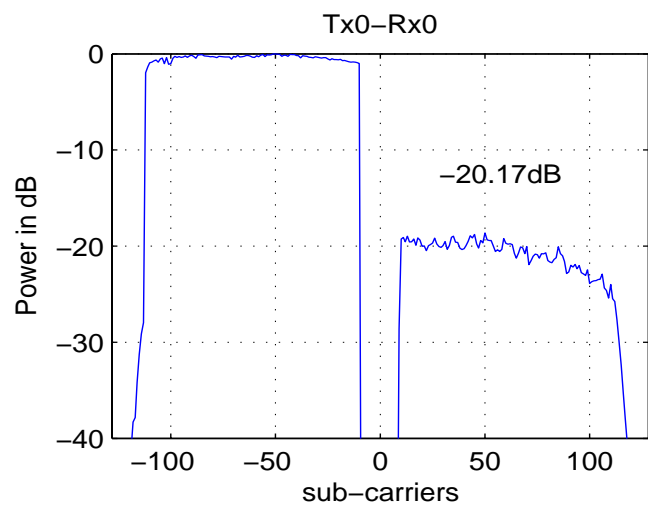


Image Suppression on the Testbed



I/Q mismatch for MIMO-OFDM

For MIMO-OFDM there is interference from the conjugate of the data on the frequency mirror subcarrier of all the datastreams.

$$\begin{bmatrix} Y_1(k) \\ Y_2(k) \\ Y_1^*(N-k) \\ Y_2^*(N-k) \end{bmatrix} = \begin{bmatrix} P_1 & Q_1 & R_1 & S_1 \\ P_2 & Q_2 & R_2 & S_2 \\ P_3 & Q_3 & R_3 & S_3 \\ P_4 & Q_4 & R_4 & S_4 \end{bmatrix} \begin{bmatrix} X_1(k) \\ X_2(k) \\ X_1^*(N-k) \\ X_2^*(N-k) \end{bmatrix} + \begin{bmatrix} V_1(k) \\ V_2(k) \\ V_1^*(N-k) \\ V_2^*(N-k) \end{bmatrix}$$

I/Q mismatch and EDOF

- EDOF measured at 10% outage and 30dB SNR. Capacity at 10% outage, 30dB SNR

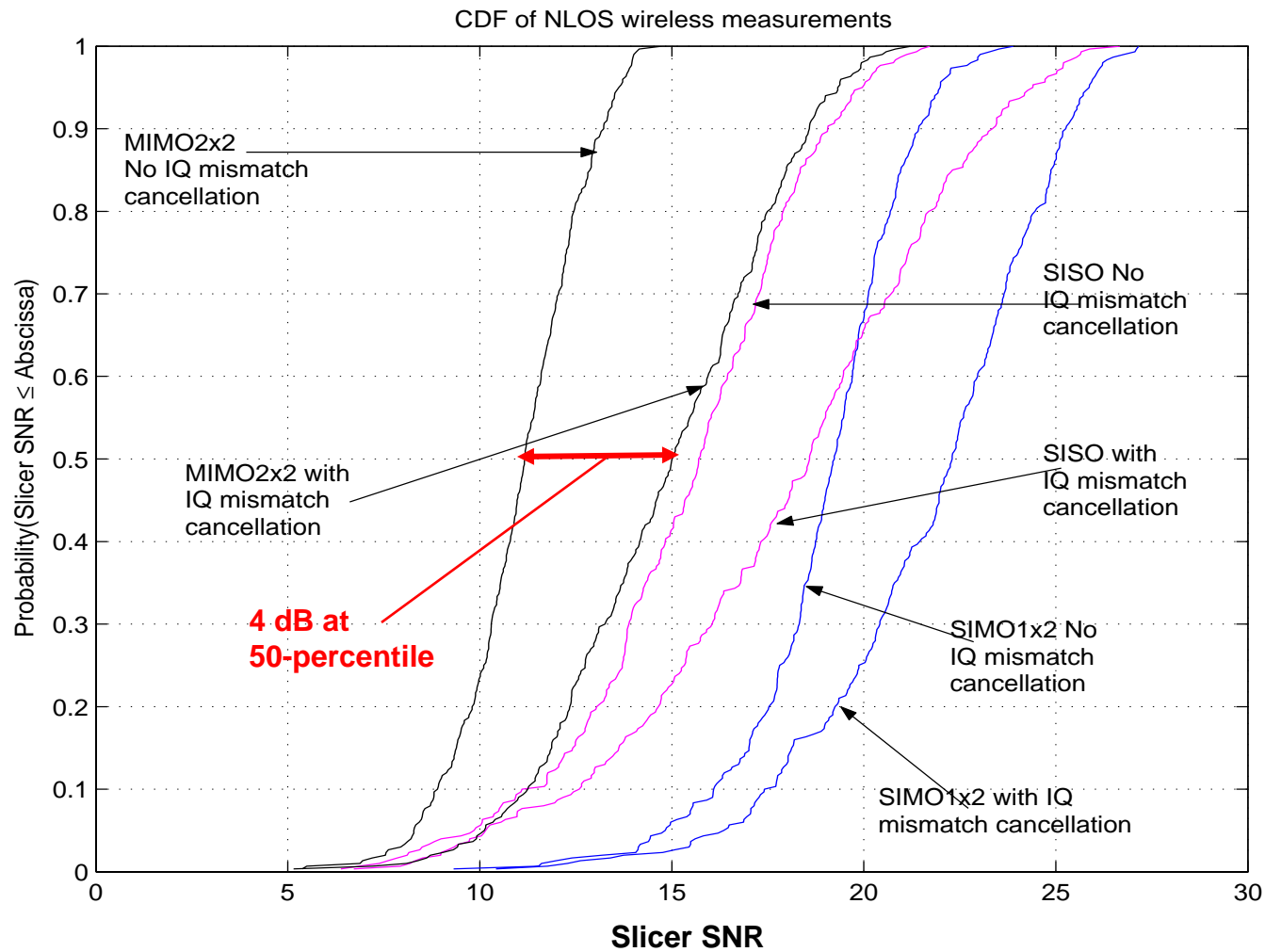
Image Suppression	-7.7dB		-10.79dB		-15.06dB		-21dB	
	EDOF	Cap.	EDOF	Cap.	EDOF	Cap.	EDOF	Cap.
1x1	0.95	9.7	0.96	10.35	0.97	10.68	0.98	11.3
2x2	1.84	21.05	1.87	22.50	1.89	23.82	1.9	25.02
2x4	1.981	28.25	1.987	30.00	1.990	31.51	1.992	32.83
4x4	3.662	45.69	3.733	48.56	3.765	51.19	3.787	53.55
8x8	7.39	93.96	7.495	99.82	7.576	105.07	7.588	109.88

- EDOF degrades slightly due to IQ mismatch !!
 - EDOF calculations use input SNR and channel estimates

$$C = \log_2(\det(I_M + \frac{\rho R}{M} H^H H)) = \sum_{k=1}^R \log_2(1 + \frac{\rho R}{M} \epsilon_k^2) \text{ bits/s/Hz}$$

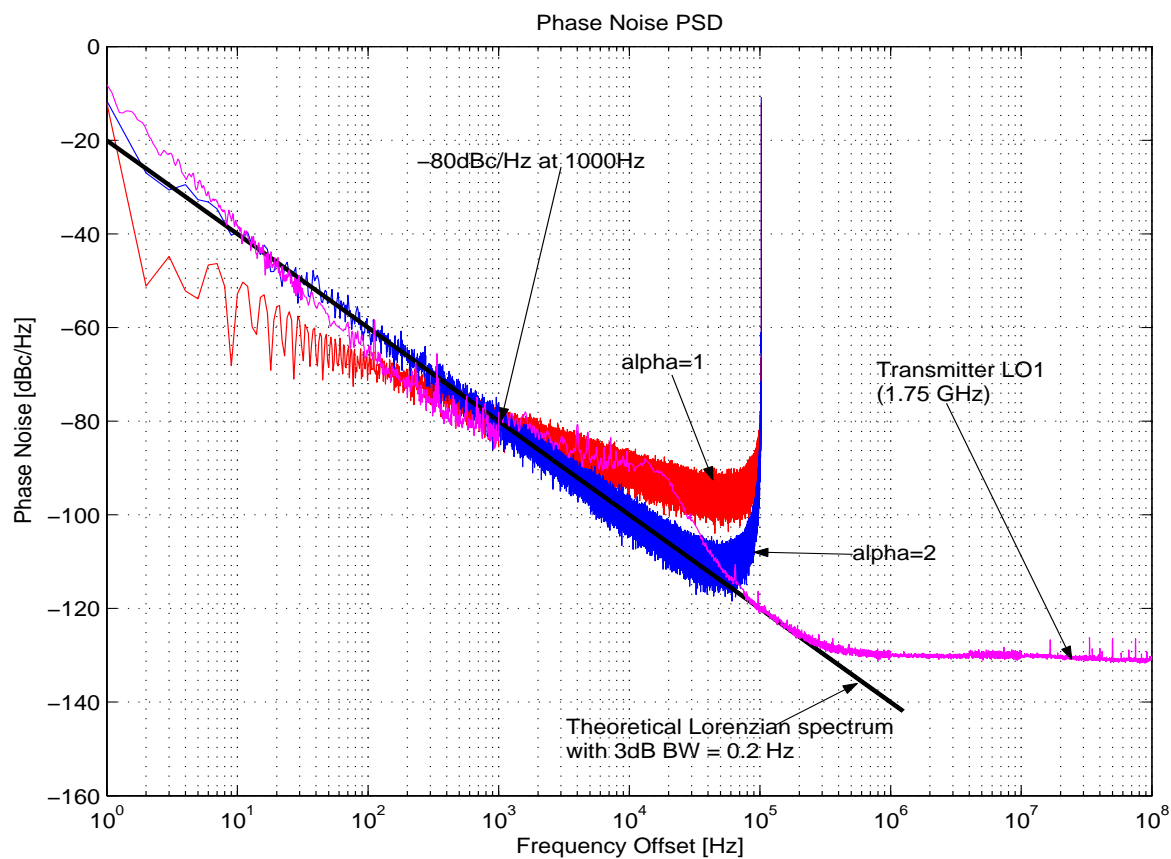
A practical definition of EDOF is the difference in capacity when ρ_R is doubled.
 EDOF = $C(2\rho_R) - C(\rho_R)$
 EDOF ranges from 0 to R

I/Q Mismatch Cancellation on the Testbed



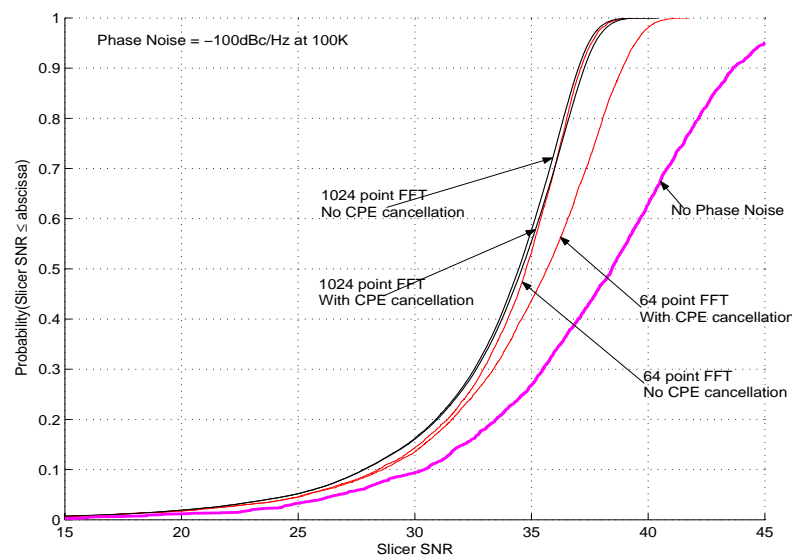
Phase Noise

Phase Noise PSD

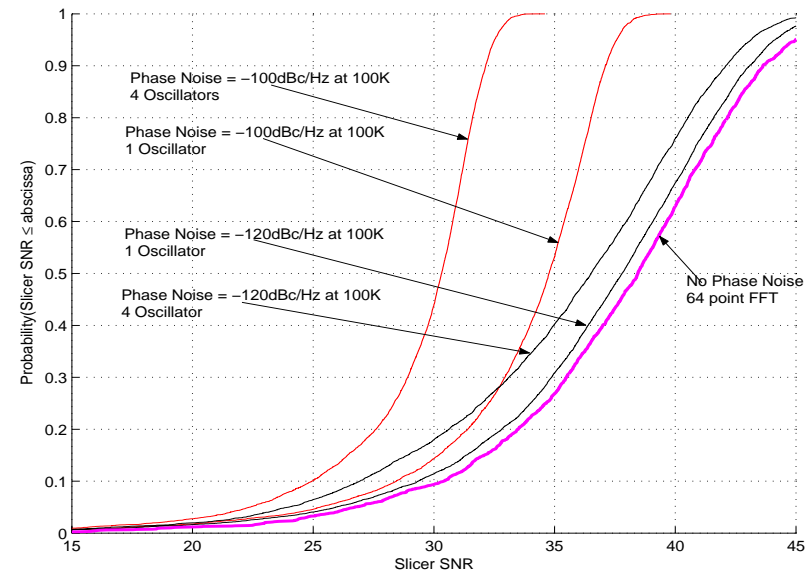


- For modeling use $1/f$ model, not $1/f^2$

Phase Noise with Varying FFT Sizes



Compare FFT sizes



Compare 1 osc and 4 osc

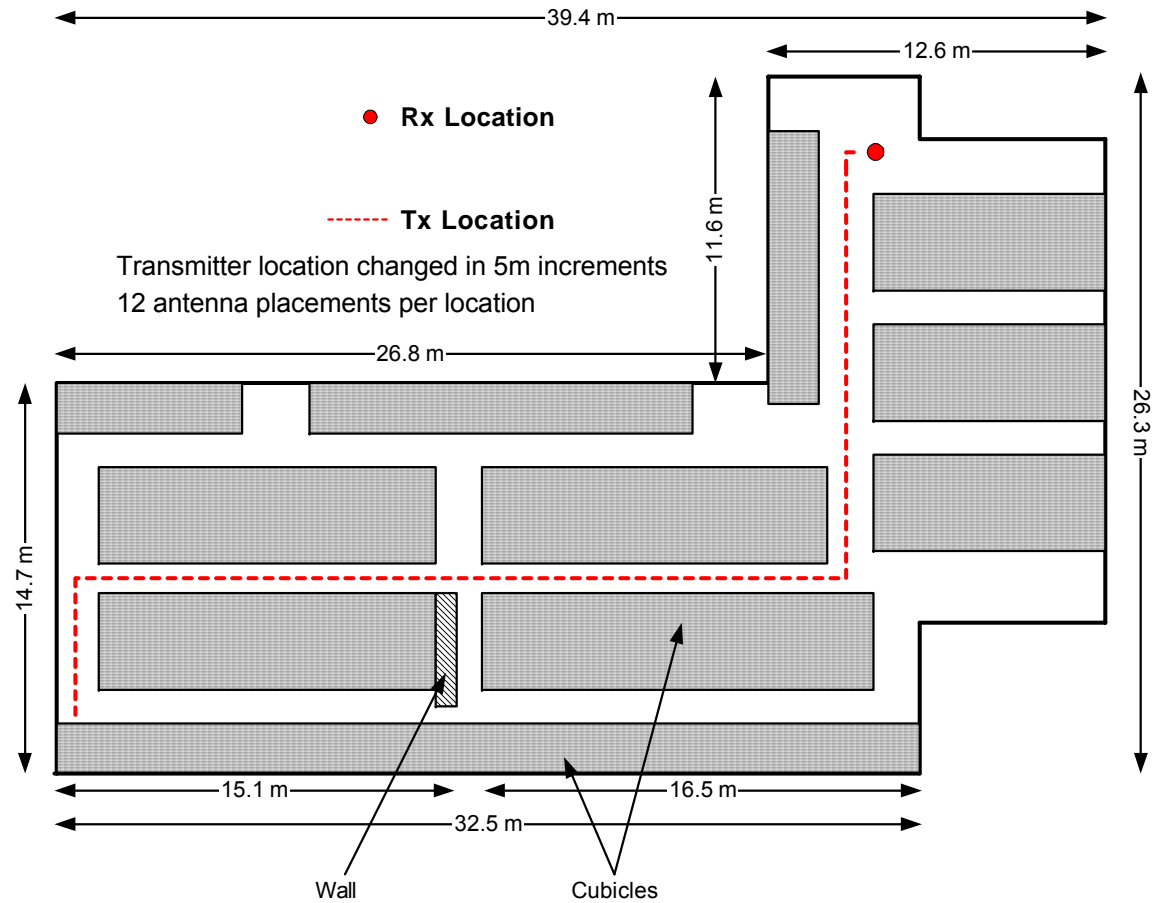
- Common phase error (CPE) decreases with increasing FFT Size
 - More difficult to eliminate with CPE cancellation
 - 1.25 dB improvement with CPE cancellation when using 64 subcarrier SISO system
- CPE decreases with increasing MIMO configuration
 - 0.75 dB to 1 dB with 2x2 64-point FFT

Experimental Measurements

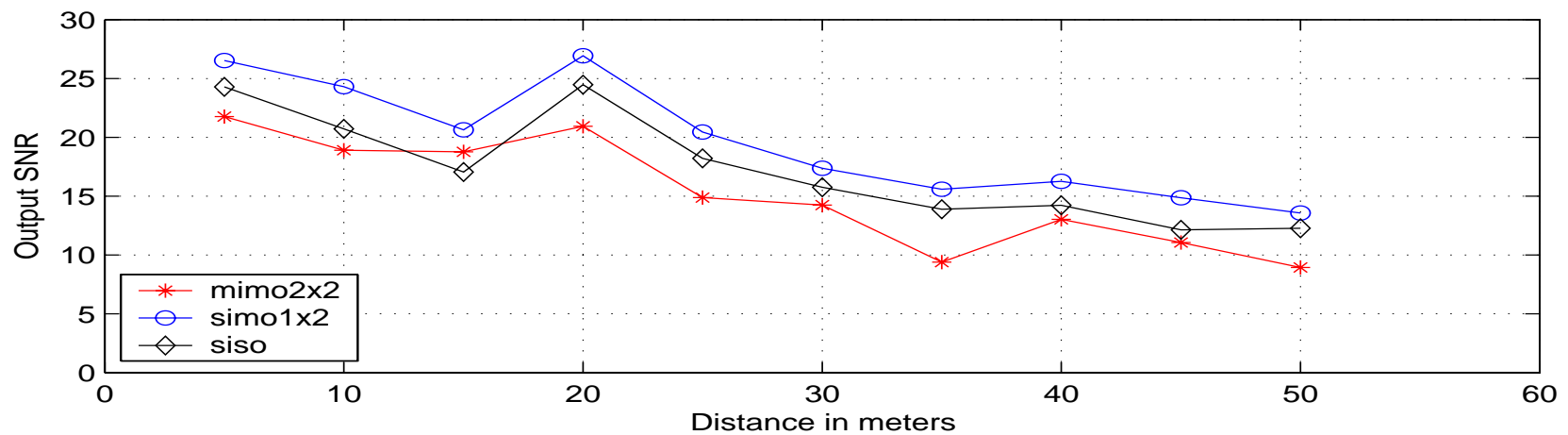
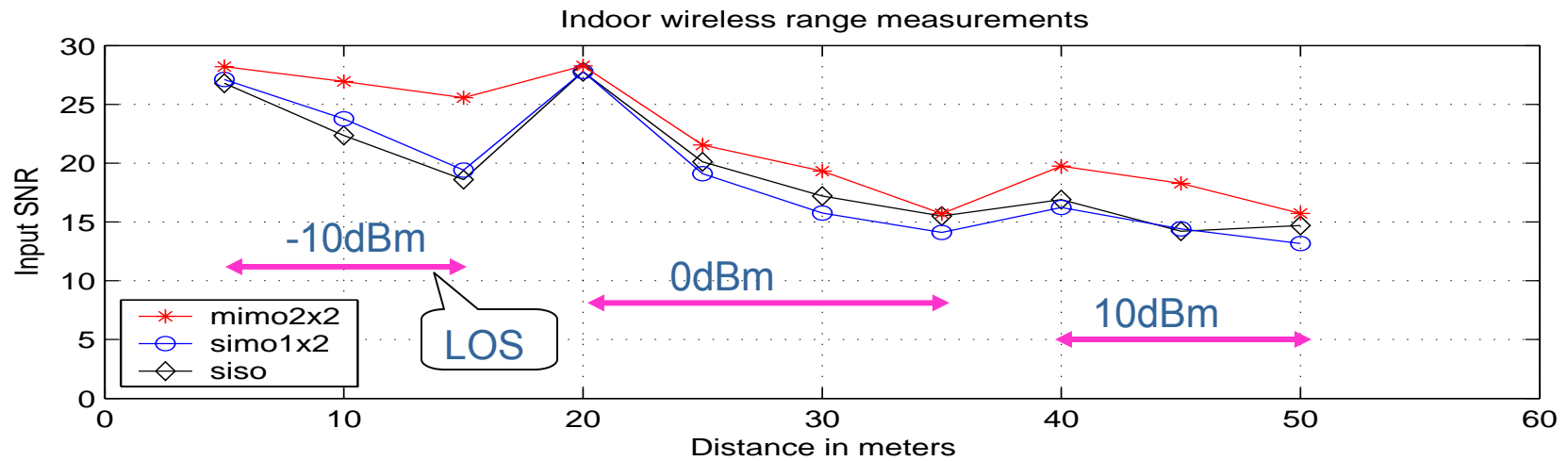
Environment 1: Cubicle Area



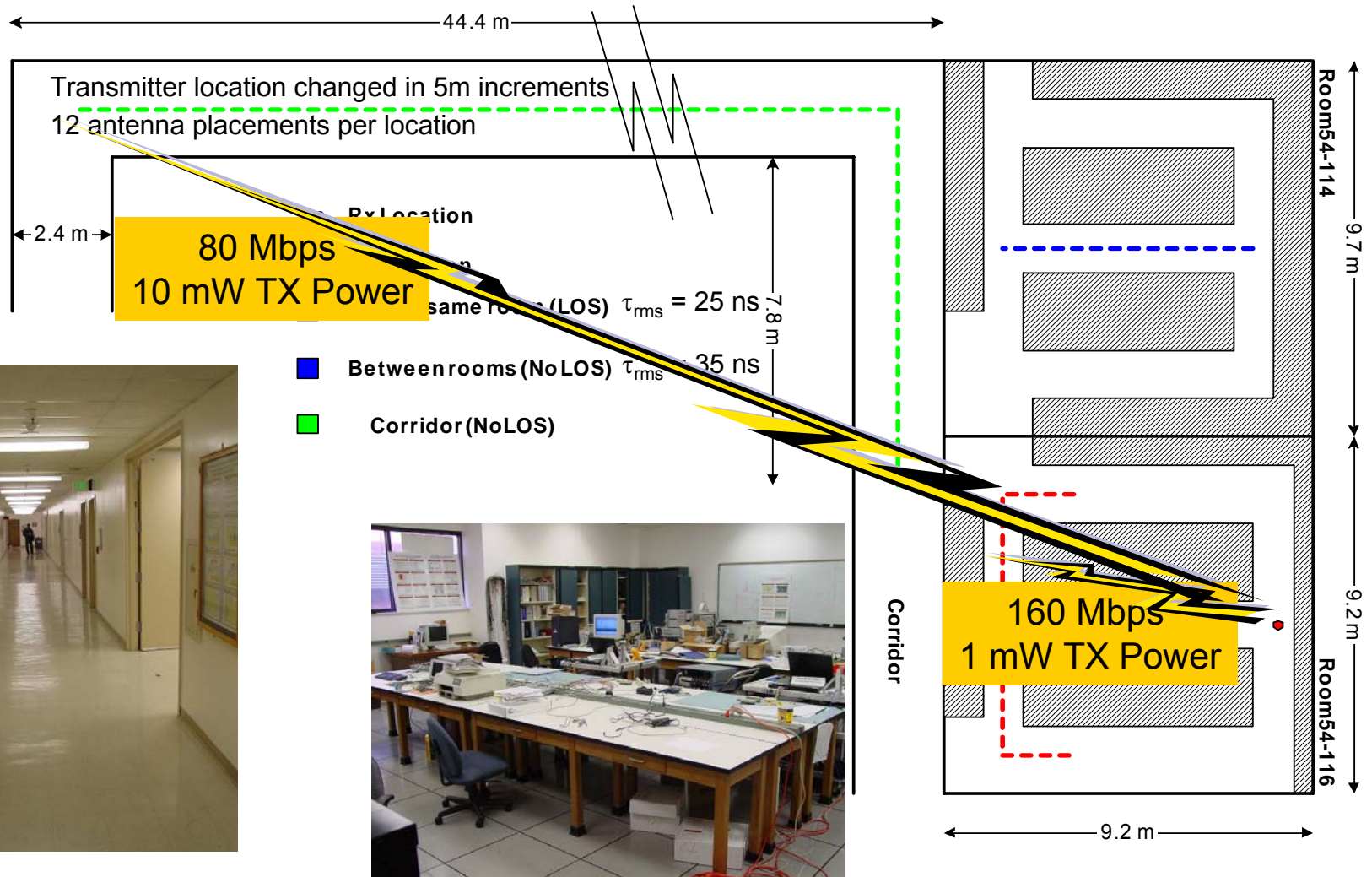
$$\tau_{rms} = 38 \text{ ns to } 50 \text{ ns}$$



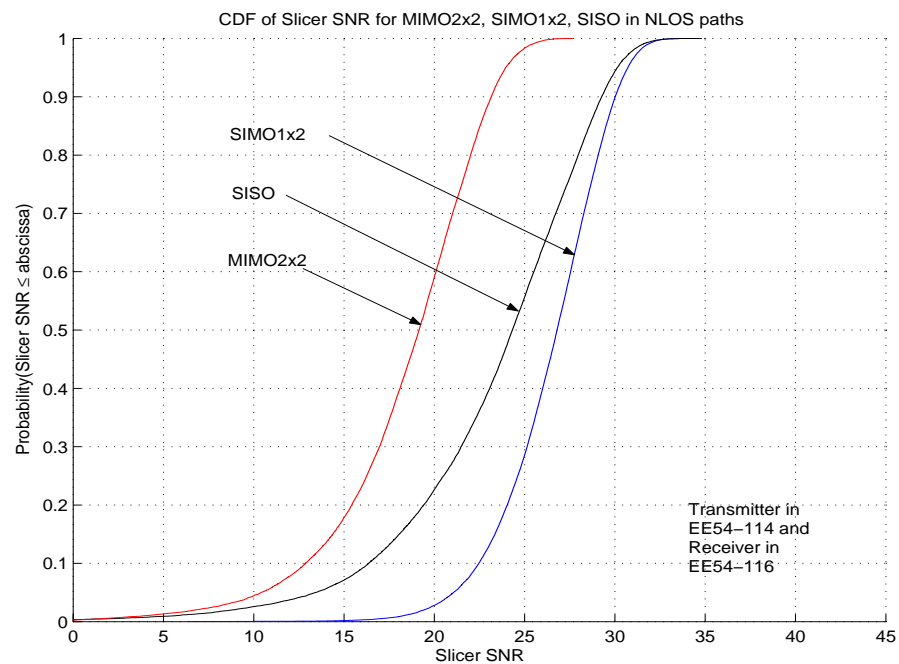
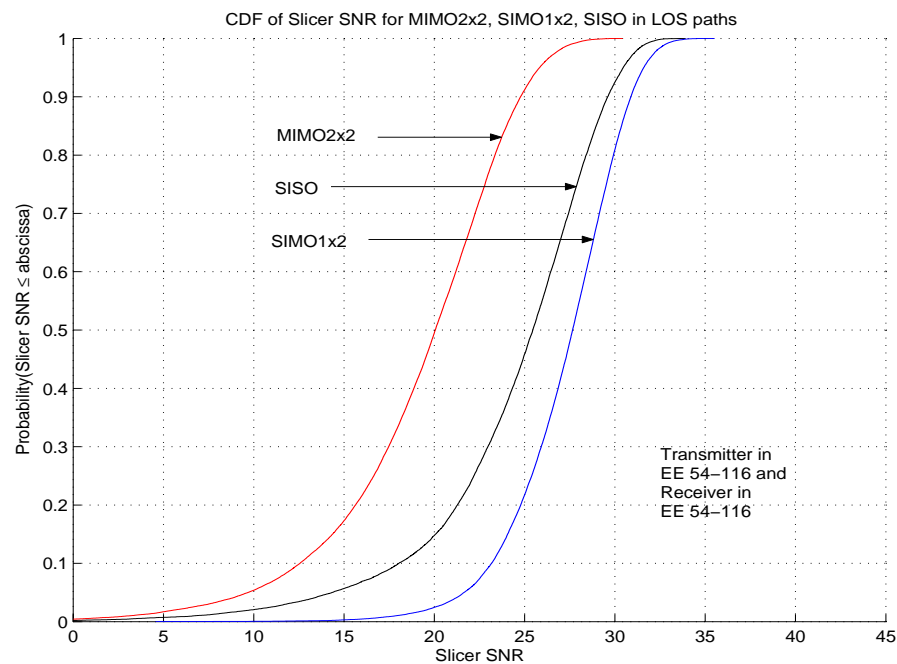
Range measurements in the cubicle area



Controlled Field Trials



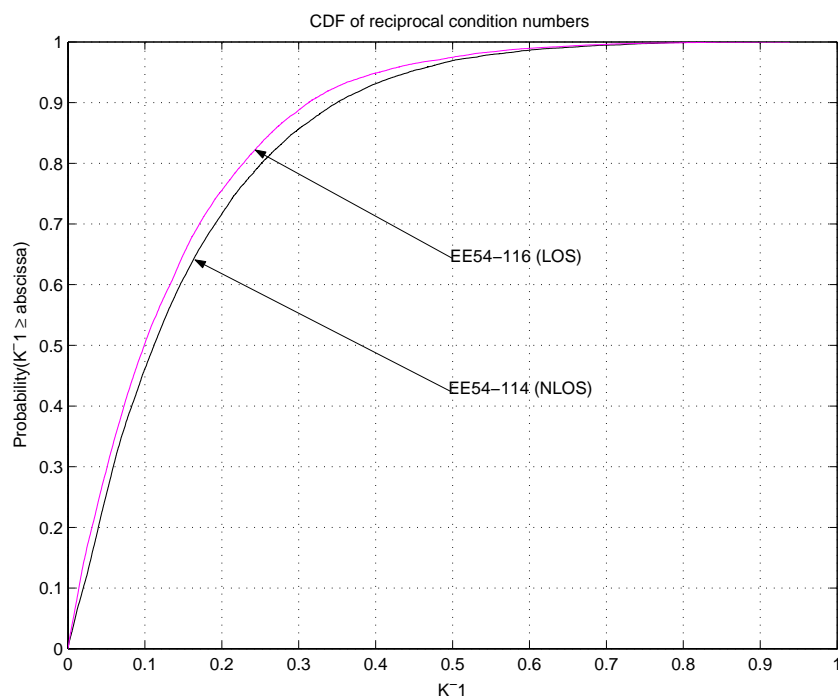
CDF of Slicer SNR for MIMO2x2, SIMO1x2 and SISO



Reciprocal condition numbers

Information theoretic Capacity

$$C = \log_2(\det(I_M + \frac{\rho_R}{M} H^H H)) = \sum_{k=1}^R \log_2(1 + \frac{\rho_R}{M} \varepsilon_k^2) \text{ bits / s / Hz}$$



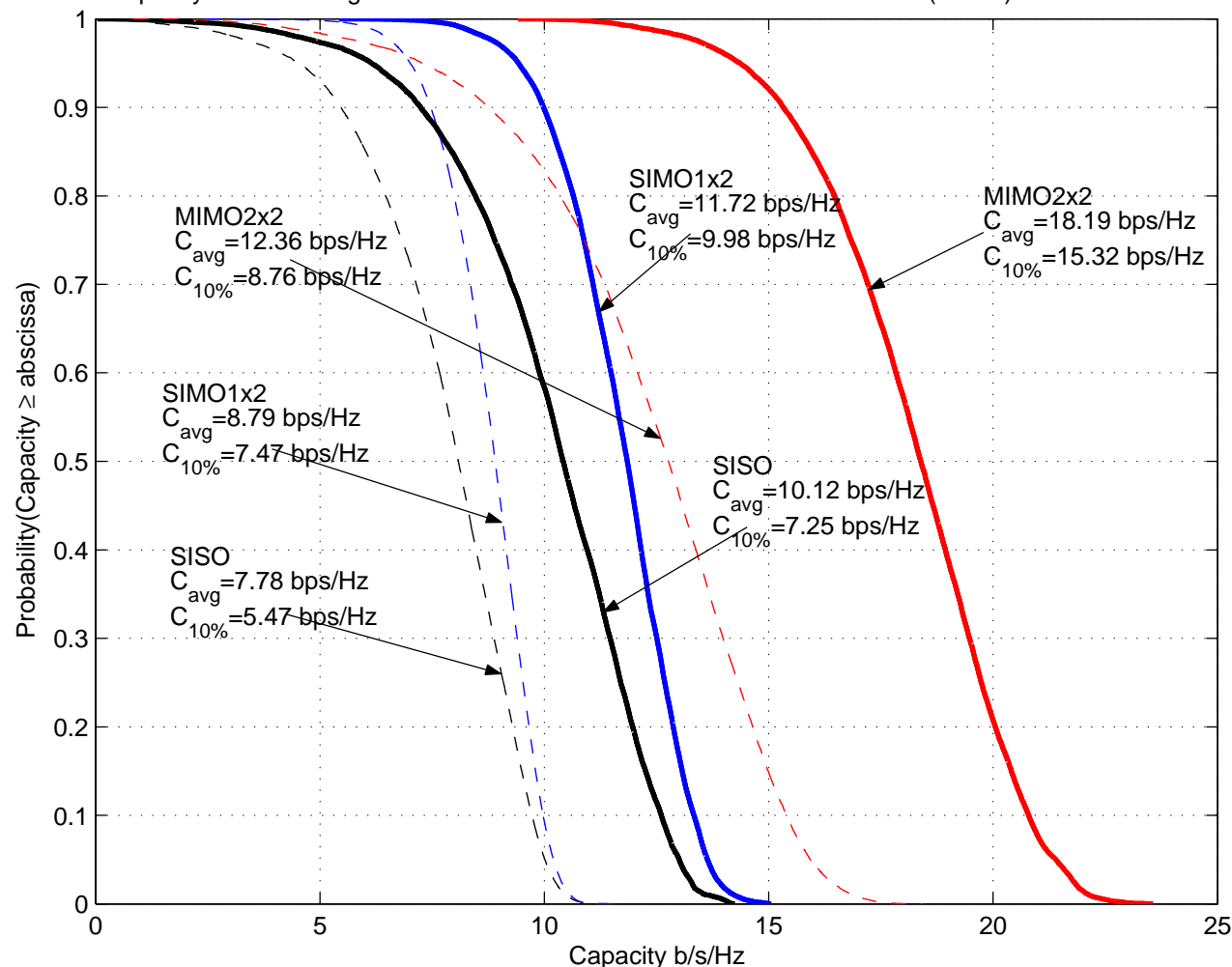
The channel matrix \mathbf{H} is an $N \times M$ matrix with rank R .
 M = num of transmit antennas
 N = num of receive antennas
 ρ_R = Received SNR,
 ε_k = singular values of \mathbf{H}

Reciprocal condition number

$$K^{-1} = \frac{\min(\varepsilon_k)}{\max(\varepsilon_k)}$$

Capacity curves in EE54-114

Capacity CCDFs using estimated channels and slicer SNR for EE54-114 (NLOS) at 30.815dB SNR



Keep received power
Constant for all cases
By referring back to the
Tx.

Theoretical channel

Capacity: ———

$$C = \log_2 \left(\det \left(I_M + \frac{\rho_R}{M} H^H H \right) \right)$$

Capacity measured
using slicer SNR

$$C_{slicer} = \log_2 (1 + SNR_{out})$$

Optimizing Overhead Using Capacity

10 symbols	15 symbols	25 symbols	35 symbols
13.15%	19.73%	32.89%	46.05%

5 pilot subcarriers	10 pilot subcarriers	20 pilot subcarriers
2.4%	4.8%	9.7%

Average capacity using slicer SNR

10 training 20 pilots	151.27 Mbps
15 training 20 pilots	144.34 Mbps
25 training 20 pilots	123.09 Mbps
35 training 20 pilots	99.36 Mbps

5 pilots 25 training	130.39 Mbps
10 pilots 25 training	128.52 Mbps
20 pilots 25 training	123.09 Mbps

10 training 5 pilots	157.66 Mbps
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RELIC – An 8x8 MIMO Detection ASIC for Wideband MIMO-OFDM System

Major Challenges for RELIC

- Wideband MIMO with high antenna count
 - Up to 8x8, 25MHz bandwidth
- Dynamic reconfiguration for
 - Different number of antennas
 - Different antenna configurations
 - Different FFT sizes
- Highly flexible packet structure support
 - including UCLA METEOR, IEEE 802.11a/g/n

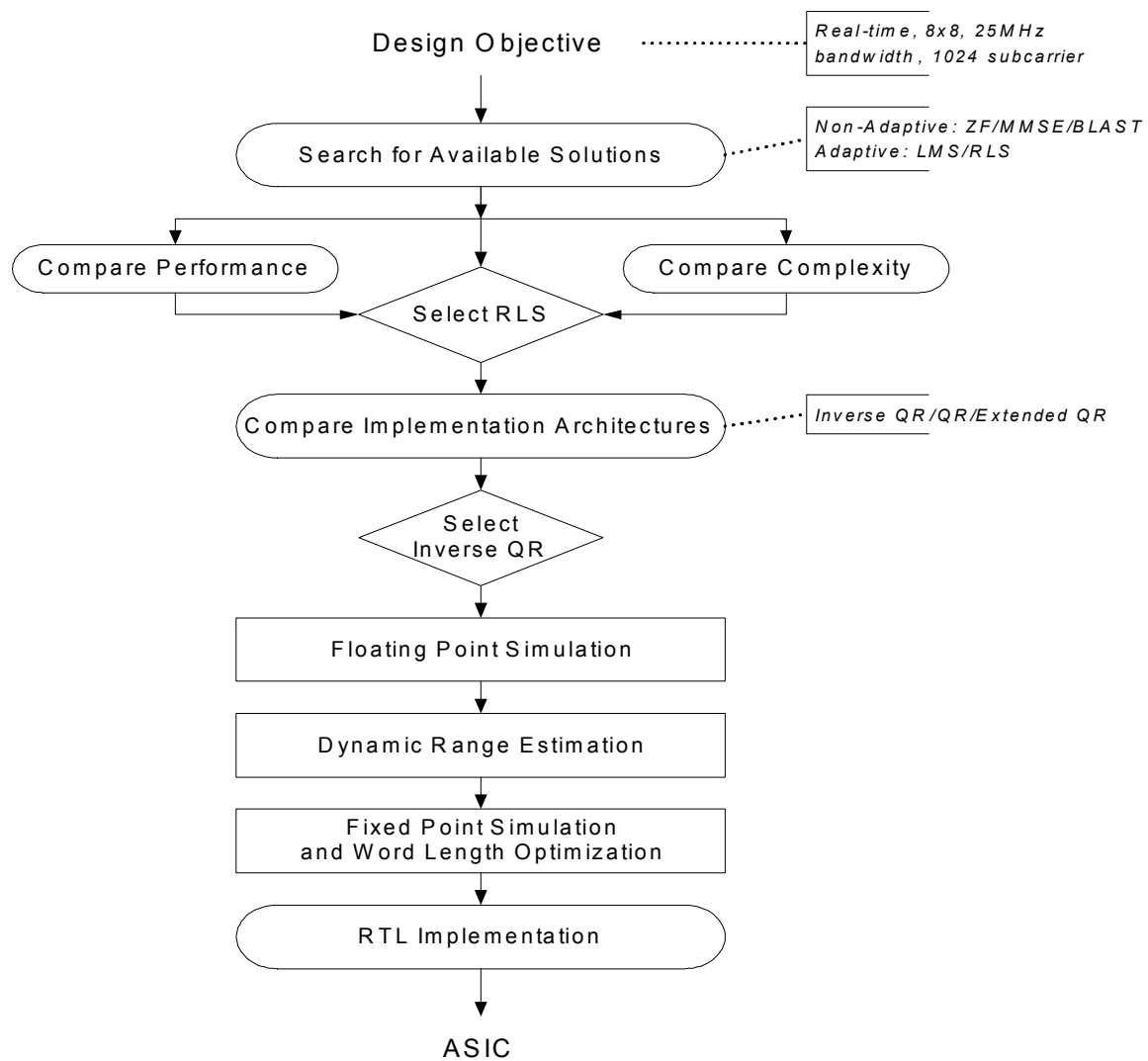
Wideband MIMO up to 8x8

- Algorithm research
 - RLS algorithm offers MMSE performance, fast convergence, and automatic adaptation to various channel conditions
- Implementation friendly architecture
 - Systolic array RLS algorithms and architectures
- Frequency domain scalability
 - Full band mode (25MHz) up to 4x4 and half band mode up to 8x8 (12.5MHz)
- Linear interpolation in frequency domain to reduce hardware complexity

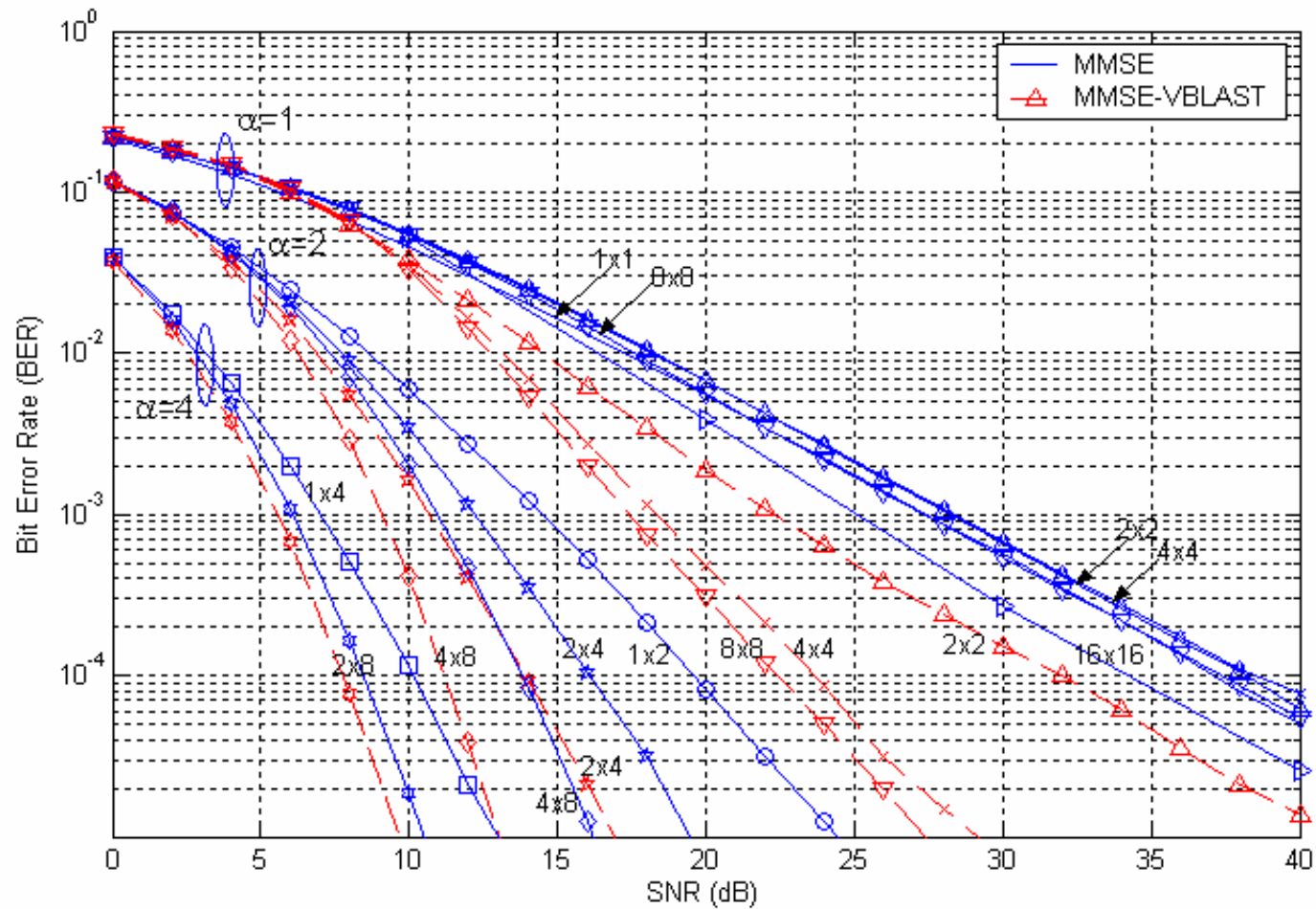
Support for Different Packet Types

- Innovative input tagging scheme
 - Supports different packet structures including UCLA METEOR and IEEE802.11a/g/n
- Real-time reconfiguration of packet structure parameters such as
 - Length of packet
 - Number of OFDM subcarriers
 - Length of training and retraining sequences

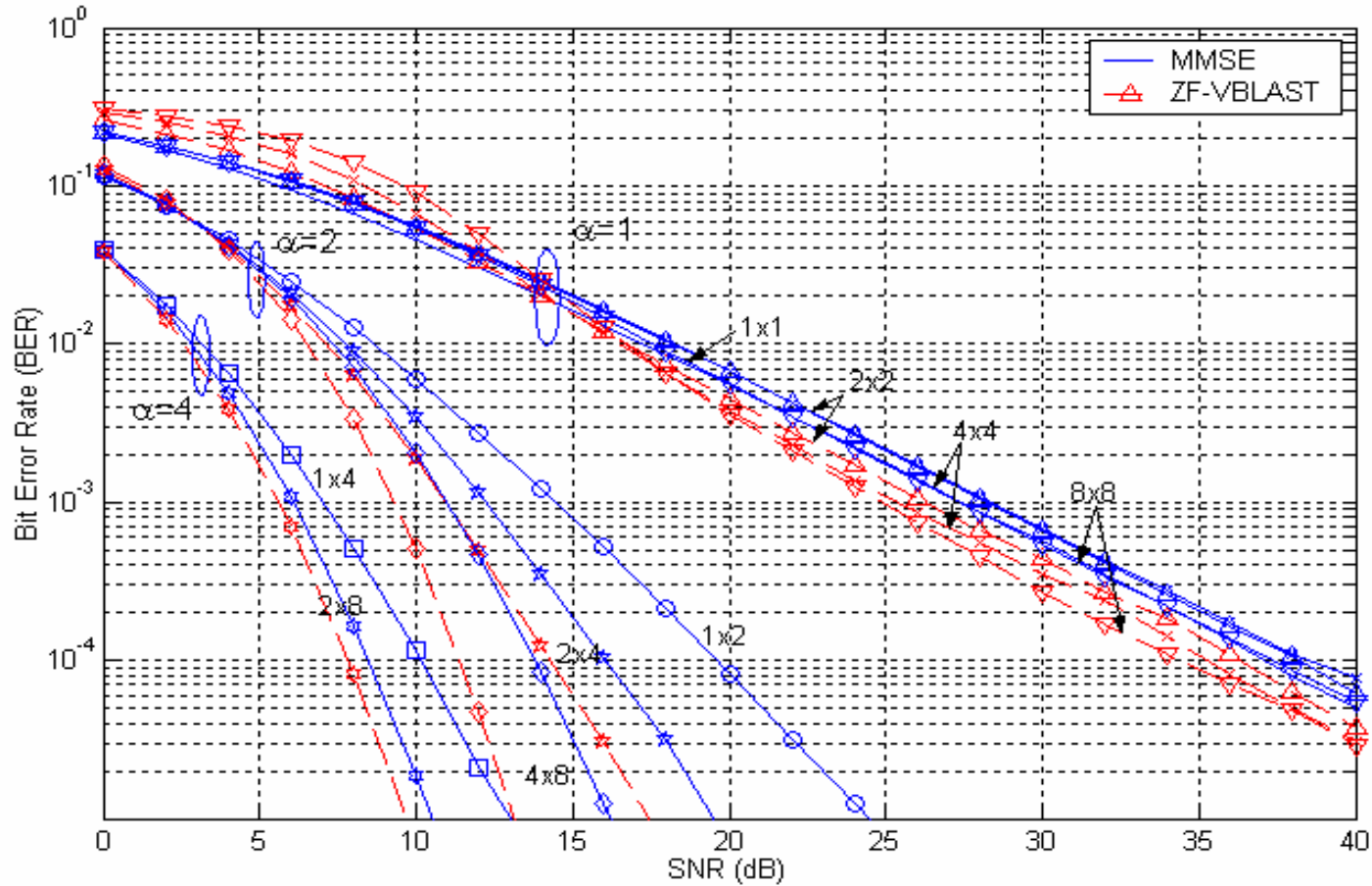
Design Process of RELIC



Simulation Results – MMSE vs. MMSE-VBLAST



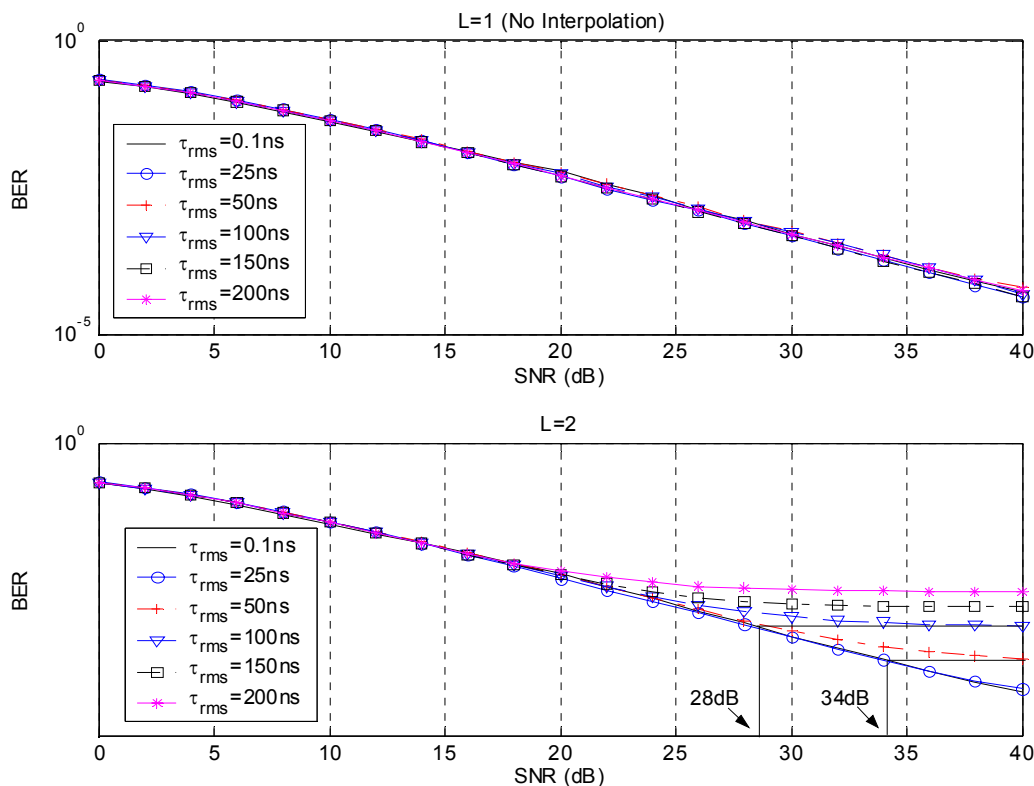
Simulation Results – MMSE vs. ZF-VBLAST



Required SNR (dB) for Uncoded $BER=10^{-3}$ (QPSK)

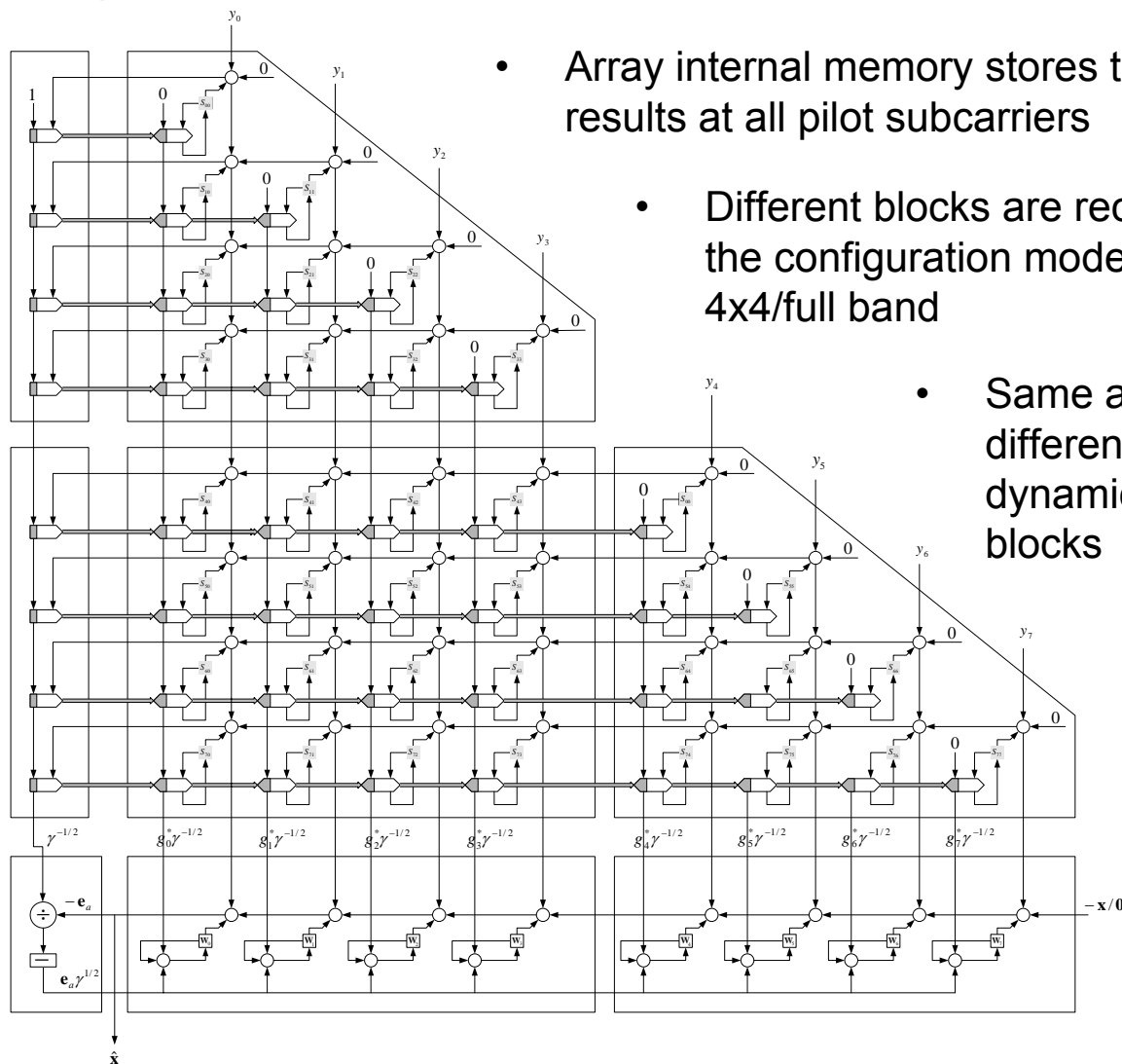
<i>N_t×N_r</i>	<i>ZF</i>	<i>MMSE</i>	<i>ZF-VBLAST</i>	<i>MMSE-VBLAST</i>
1×1	27.4	27.4	27.4	27.4
2×2	29.9	28.2	25.4	18.3
4×4	33.1	28.3	25.4	18.3
8×8	36.0	27.3	24.8	17.4
1×2	14.4	14.4	14.4	14.4
2×4	12.5	12.2	11.0	10.7
4×8	11.4	11.0	9.3	9.1
1×4	7.0	7.0	7.0	7.0
2×8	6.2	6.1	5.6	6.5

Channel RMS Delay Spread vs. Interpolation ($N_c=256, 1 \times 1$)



- When $L=1$, the BER floor in $N_c=64$ case has disappeared because the cyclic prefix length is sufficiently long (2560ns for $N_c=256$)
- When $L=2$, the floor is:
 - @ $\tau_{rms}=50\text{ns}$:
 $SNR_{max}=34\text{dB}$,
 $BER_{min}=0.02\%$,
 - @ $\tau_{rms}=100\text{ns}$:
 $SNR_{max}=28\text{dB}$,
 $BER_{min}=0.07\%$

A Fully Pipelined Inverse QR-RLS Architecture for OFDM



- Array internal memory stores the QR decomposition results at all pilot subcarriers
- Different blocks are reconnected according to the configuration mode, i.e. 8x8/half band, or 4x4/full band
- Same architecture supports all different antenna setups by dynamically connecting different blocks
- Combining array has been mapped onto a linear array by timing multiplexing

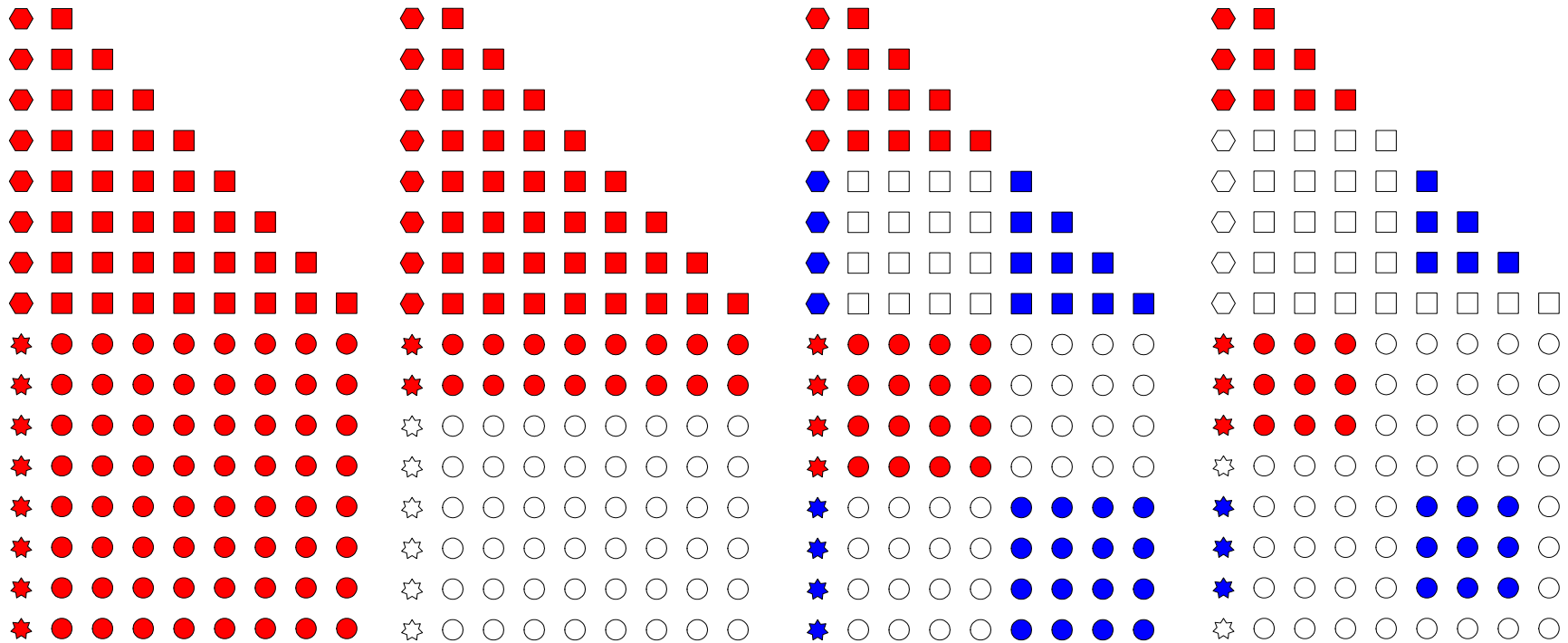
Topology of Different Configuration

8x8 @ 12.5MHz

2x8 @ 12.5MHz

4x4 @ 25MHz

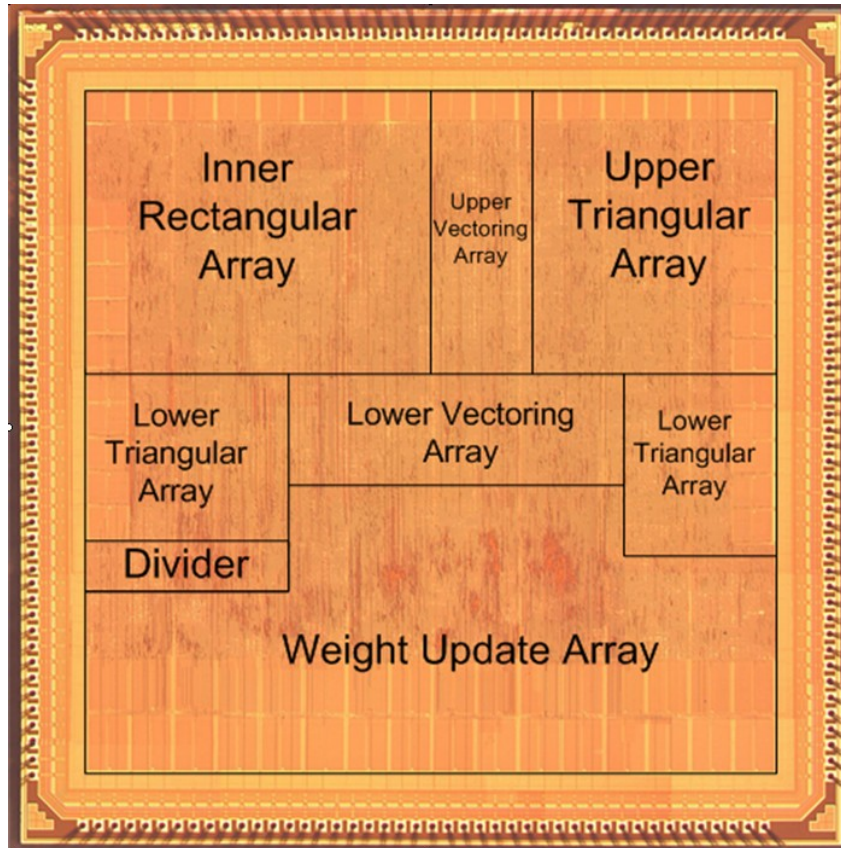
3x3 @ 25MHz



RELIC Specifications

- Maximum clock frequency: 50 MHz
- Supported antenna setup: any valid combination of antennas ($N_t \leq N_r$) up to 8x8
- Dual modes
 - Full band (25MHz): up to 4x4 with 1024 subcarriers
 - Half band (12.5MHz): up to 8x8 with 512 subcarriers and expandable to full band with two RELIC chips
- Real-time (packet-wise reconfigurable) receive antenna selection (soft switching)
- Extremely flexible architecture that can be easily adapted to different OFDM packet structures

RELIC Die Microphotograph



- Process: TSMC 0.18um CMOS, 3.3V/1.8V
- Die Size: 39.4mm² (core: 29.2mm²)
- Gate Count: 2.3M (SRAM: 819Kb)
- Packaging: 181-lead PGA
- Power: 360mW (@58MHz, 2x2)
- Clock Freq: 50MHz (max: 58MHz)